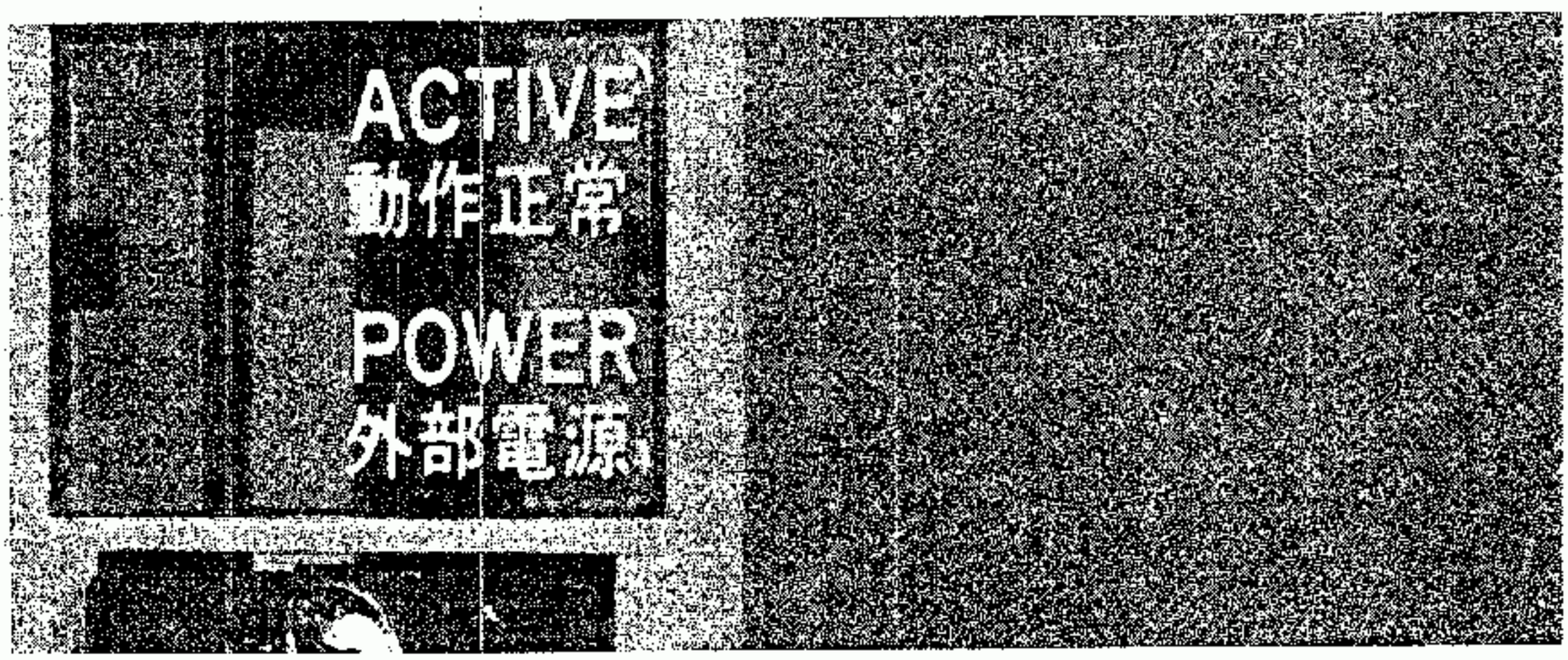
1000 Series Counter Modules

FOR Memocon-SC R84H, U84, U84J, 584

TYPES JAMSC-B1081C, -B1082C



YASKAWA

1. INTRODUCTION

This manual describes the functions and the operation of the 1000 Series Counter Modules (in this manual, called module). For the functions and operations of Programmable Controller, refer to the following PC user's manuals:

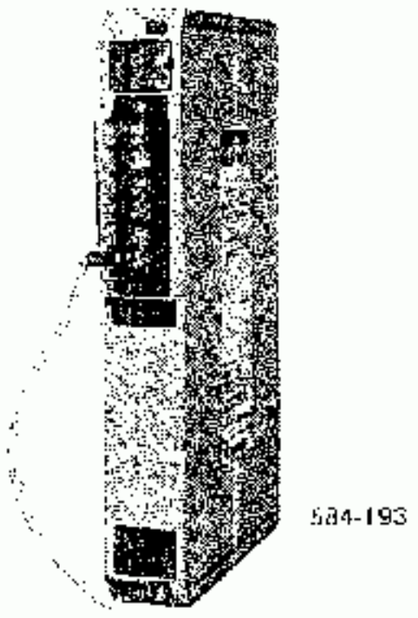
- Memocon-SC R84H – SIE-C815-9.4
- Memocon-SC U84 – SIE-C815-10.1
- Memocon-SC 584 – SIE-C815-7

The module is in two types: reversible counter module (type JAMSC-B1081C) and preset counter module (type JAMSC-B1082C). See Fig. 1.1.

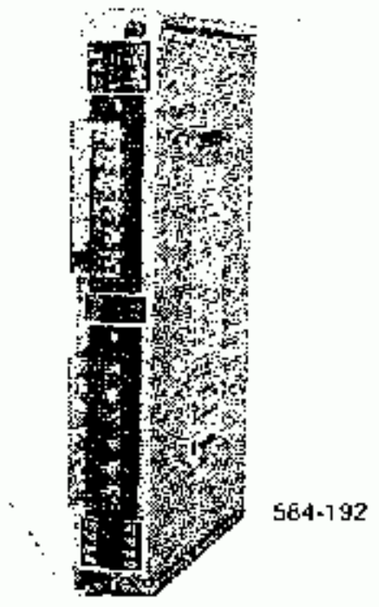
B1081C counts incoming high-speed pulses (max. 40 kpps), and sends the counts at every scan of the mainframe to the mainframe. B1082C has all of the capabilities of B1081C plus a notch output capability. When notch point set values are given by the mainframe, the module compares the counts against the set notch point values, and outputs notch signals continuously. Memocon-SC R84H, U84, U84J and 584 can be used as the mainframe.

This module has the following features, and can be used widely to count high-speed pulses for a variety of positioning controls in manufacturing industries.

- Counts up to 6 digits in decimal.
- Number of digits expandable by carrying and borrowing.
- Up to 8 notch points in 6-digit decimals can be set (only with B1082C).
- Simple count checking by count test input.
- Self-diagnostic function to ensure high reliability.



(a) Reversible Counter
Type JAMSC-B1081C



(b) Preset Counter
Type JAMSC-B1082C

Fig. 1.1 Counter Modules

CONTENTS

2. REVERSIBLE COUNTER (TYPE JAMSC-B1081C)

2.1 SUMMARY

Fig. 2.1 shows the exterior view of B1081C. B1081C is mounted on the mounting base of 1000 series I/O. It is the same size as one normal discrete I/O module (1 span) of the 1000 series I/O, and can be inserted in any of the slots in the mounting base.

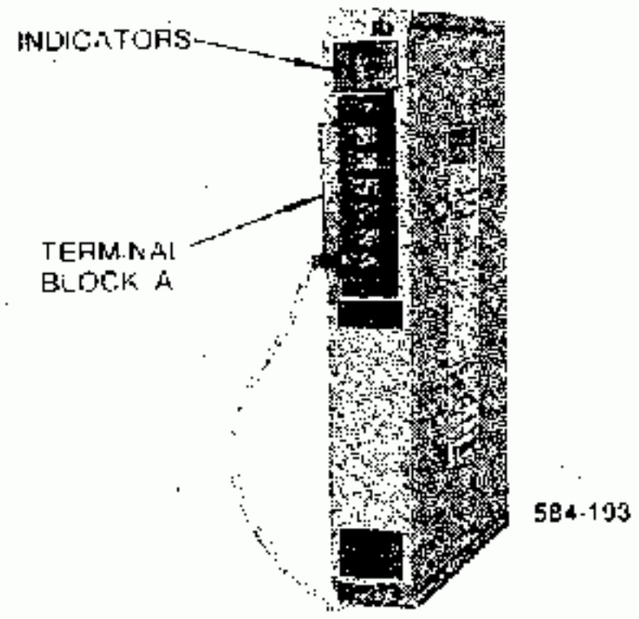


Fig. 2.1 Exterior View of B1081C

The external wiring terminal block and the indicator lamps are located on the front face of the module. The external wiring terminal block has 12 pins, and up to two 1.25mm^2 wires can be connected to each pin. The terminal block is attached to the module with two screws, so that when the module is to be replaced, only these two screws need to be removed without the individual wires being disconnected. The setting switches on the left side of the module are for selection of the pulse modes.

Fig. 2.2 shows the block diagram of B1081C. As input pulses, either two-phase or single-phase-with-sign pulses can be used, and as pulse count scaling, single or double counting mode can be selected with the setting switch. For counting low speed pulses with high noise content, low input pulse rates (400 pps) can be selected with the setting switch.

In addition, external input signals $\overline{\text{COUNT ENABLE}}$ / $\overline{\text{EXTERNAL RESET}}$ and $\overline{\text{ADDITION TEST}}$ and $\overline{\text{SUBTRACT TEST}}$ signals can be accomodated. With the latter two, the current module values can be increased or decreased without inputting external pulses, for convenient checking during test run or trouble-shooting.

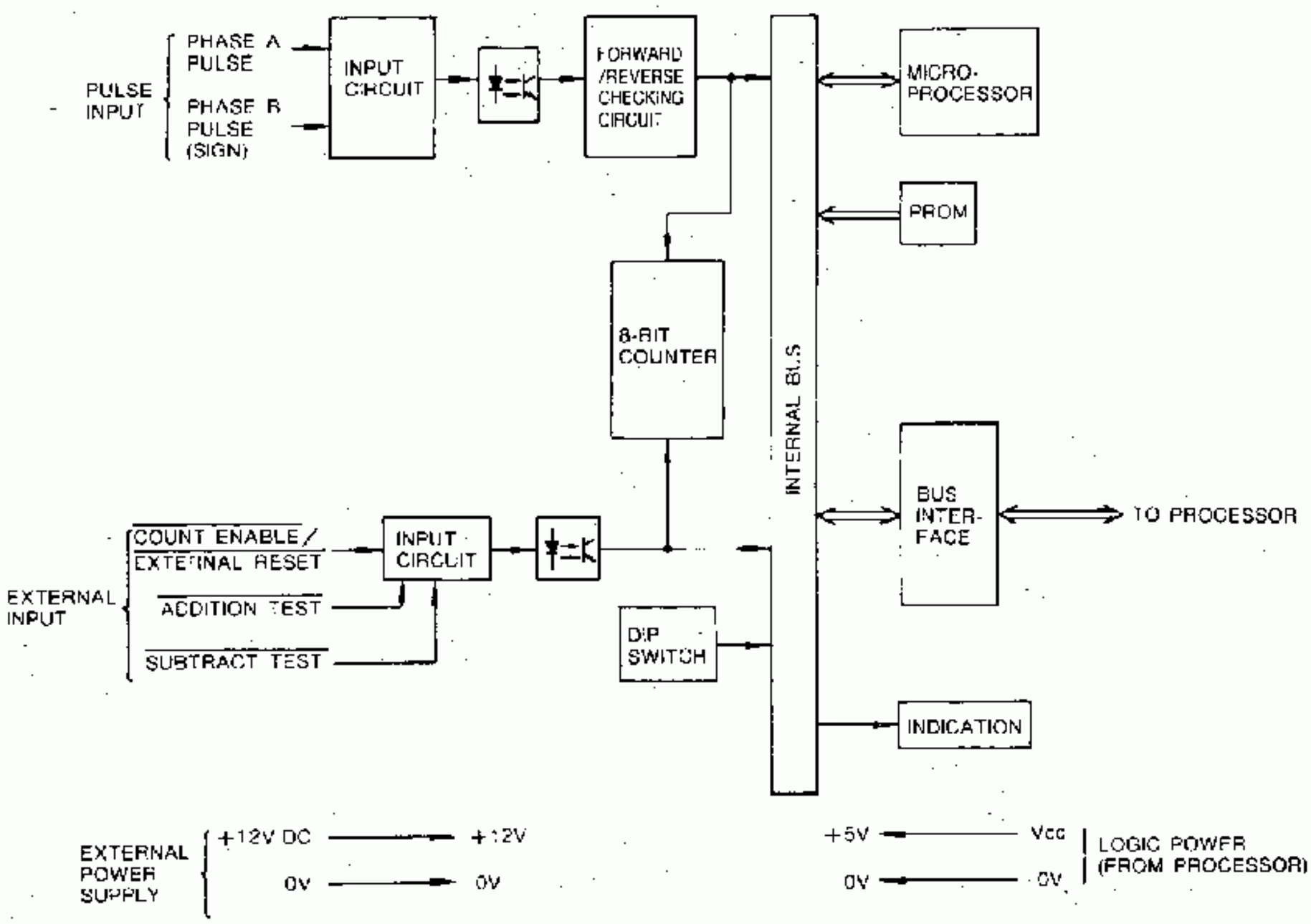


Fig. 2.2 Block Diagram of B1081C

2. 2 SPECIFICATIONS

Table 2. 1 Specifications

Item	Specification
Name	Revers ble counter modu e
Type	JAMSC-B1081 C
Ambient Temperature	0 to +55 ℃
Storage Temperature	−20 ℃ to +85 ℃
Humidity	5 % to 95 % RH (non-condensing)
Vibration Resistance	In compliance with JIS* C 0911
Shock Resistance	10 G max.
Environmental Condition	Free from explosive, inflammable and corrosive gases.
Dielectric Strength	500 VDC
Number of Circuits	1 circuit/module
Mainframes	*Memocon-SC* R84H, U84, U84J, 584
Number of Digits	Decimal 6 digits for R84H and 8 digits for U84, U84J. 584
Max. Counting Speed	40 kpps or 400 pps (switchable)
Input Pulse Mode	2-phase or single-phase-with-sign (switchable)
Pulse Count Multiplier	×1 or ×2 (switchable)
Heating Value	10 W max
External Power Supply	+12 VDC ⊥10 %, 0.1 A max.
Dimensions in mm	34.5 (W) × 250 (H) × 99 (D)
Approx. Weight	0.8 kg

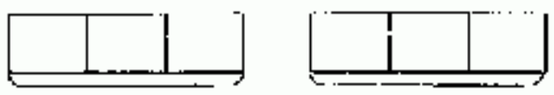
*Japanese Industrial Standard

2. 3 INTERNAL INTERFACE (SIGNAL COMMUNICATION WITH R84H)

2. 3. 1 Module to R84H

(1) Current Value of Counter

The current value of the counter is input to two consecutive input registers (30××, 30×× + 1) in 6-digit decimals. The input registers to be used are determined by the R84H I/O allocation.



High-order 3 digits — Low-order 3 digits — 6-digit decimal

30×× — 30×× + 1 — 0 - 999999

(2) Control Signal

Table 2. 2 shows the outline of the control signals (discrete input relay).

Table 2. 2 Control Signal (Discrete Input Relay) Outline

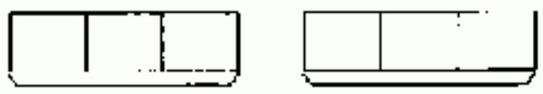
Input Relay Number	Name	Description
1001 + 8n	READY	Module self-diagnostic results. ON means normal, and OFF means abnormal. OFF for approx 0.5 s at power ON or module reset.
1002 + 8n	CARRY	When current value of counter exceeds 999999 and becomes 000000, turned on for one scan.
1003 + 8n	BORROW	When current value of counter decreases from 000000 (negative) and becomes 999999, turned on for one scan.
1004 + 8n		Not used.
1005 + 8n		
1006 + 8n		
1007 + 8n		
1008 + 8n		

Note:
1. n = 0 to 31.
2. Input relays 1004 + 8n to 1008 + 8n cannot be used for other applications.

2. 3. 2 R84H to Module

(1) Presetting of Current Values

To preset the current value in a 6-digit decimal from the R84H to the module, two consecutive output registers (40××, 40×× + 1) are used. The output registers to be used are determined by the R84H I/O allocation



High-order 3 digits — Low-order 3 digits — 6-digit decimal

40×× — 40×× + 1 — 0 - 999999

(2) Control Signal

Table 2. 3 shows the outline of the control signals (discrete output coil).

Table 2. 3 Control Signal (Discrete Output Coil) Outline

Output Coil Number	Name	Description
0001 + 8n	MODULE RESET	When MODULE RESET changes from OFF to ON, the module starts the same power up process as at the initial power switching on time, and initializes itself. Possible in 1-scan ON. Effective all the time.
0002 + 8n	CURRENT VALUE RESET	While CURRENT VALUE RESET is ON, the current value of counter is kept cleared Possible in 1-scan ON. Always effective.
0003 + 8n	ENABLE	While ENABLE is ON, current value counting is possible, and pulse input can be accepted. While ENABLE is OFF, these functions are disabled
0004 + 8n	PRESET REFERENCE	When PRESET REFERENCE is turned ON, the current value is preset. Always effective.
0005 + 8n		Not used.
0006 + 8n		
0007 + 8n		
0008 + 8n		

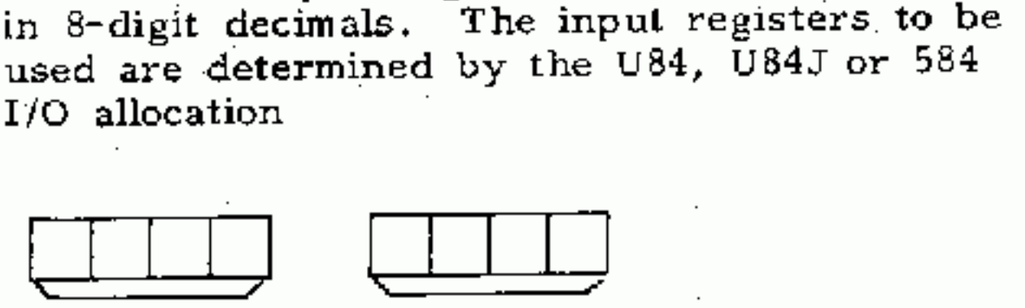
Note:
1. n = 0 to 31.
2. Output coils 0005 + 8n to 0008 + 8n are available as internal coils of R84H.

2.4 INTERNAL INTERFACE (SIGNAL COMMUNICATION WITH U84, U84J, 584)

2.4.1 Module to U84, U84J, 584

(1) Current Value of Counter

The current value of the counter is input to two consecutive input registers (3××××, 3×××× +1) in 8-digit decimals. The input registers to be used are determined by the U84, U84J or 584 I/O allocation



High-order 4 digits	Low-order 4 digits	8-digit decimal
3××××	3×××× +1	0 - 99999999

(2) Control Signal (Discrete Input Relay)

Table 2.4 shows the outline of the control signals (discrete input relay).

Table 2.4 Control Signal (Discrete Input Relay) Outline

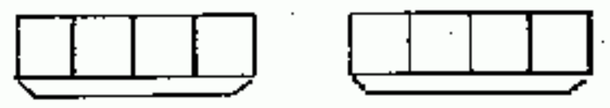
Input Relay Number	Name	Description
10001+8n (10001+16n)	READY	Module self-diagnostic results ON means normal, and OFF means abnormal. OFF for approx 0.5 s at power ON or module reset.
10002+8n (10002+16n)	CARRY	When current value of counter exceeds 99999999 and becomes 00000000, turned on for one scan.
10003+8n (10003+16n)	BORROW	When current value of counter decreases from 00000000 (negative) and becomes 99999999, turned on for one scan.
10004+8n (10004+16n) to 10008+8n (10016+16n)	Not used.	

Note:
1. n=0, 1, 2·····
2. Input relay numbers in ( ) show those of the 584.
3. The following input relay numbers cannot be used for other applications:
   - 10004+8n to 10008+8n for U84 and U84J
   - 10004+16n to 10016−16n for 584

2.4.2 U84, U84J, 584 to Module

(1) Presetting of Current Values

To preset the current value in a 8-digits decimal from the U84, the U84J or the 584 to the module, two consecutive output registers (4××××, 4××××+1) are used. The output registers to be used are determined by the U84, the U84J or the 584 I/O allocation.



High-order 4 digits	Low-order 4 digits	8-digit decimal
4××××	4××××+1	0 - 99999999

(2) Control Signal

Table 2.5 shows the outline of the control signals (discrete output coil).

Table 2.5 Control Signal (Discrete Output Coil) Outline

Output Coil Number	Name	Description
00001+8n (00001+16n)	MODULE RESET	When MODULE RESET changes from OFF to ON, the module starts the same power up process as at the initial power switching on time, and initializes itself. Possible in 1-scan ON. Effective all the time.
00002+8n (00002+16n)	CURRENT VALUE RESET	While CURRENT VALUE RESET is ON, the current value of counter is kept cleared. Possible in 1-scan ON. Always effective.
00003+8n (00003+16n)	ENABLE	While ENABLE is ON, current value counting is possible, and pulse input can be accepted. While ENABLE is OFF, these functions are disabled.
00004+8n (00004+16n)	PRESET REFERENCE	When PRESET REFERENCE is turned ON, the current value is preset. Always effective.
00005+8n (00005+16n) to 00008+8n (00016+16n)	Not used.	

Note:
1. n=0, 1, 2·····
2. Output coil numbers in ( ) show those of the 584.
3. The following output coil numbers are available as internal coils of U84, U84J or 584:
   - 00005+8n to 00008+8n for U84 and U84J.
   - 00005+16n to 00016+16n for 584

2. 5 EXTERNAL INTERFACE

2. 5. 1 Input Signal

(Fig. 2. 3, Tables 2. 6, 2. 7, 2. 8)

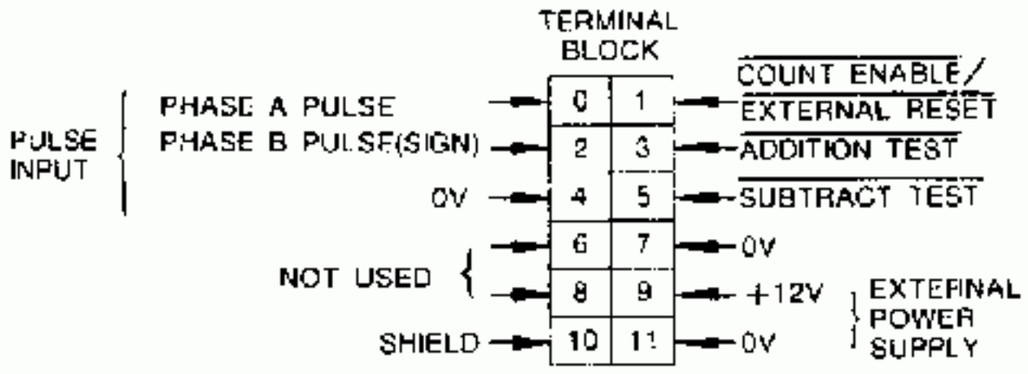


Fig. 2. 3 Input Terminal Layout

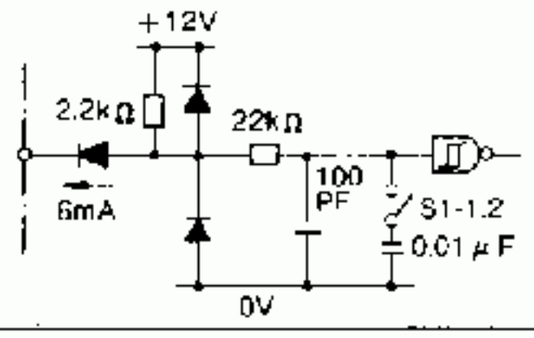
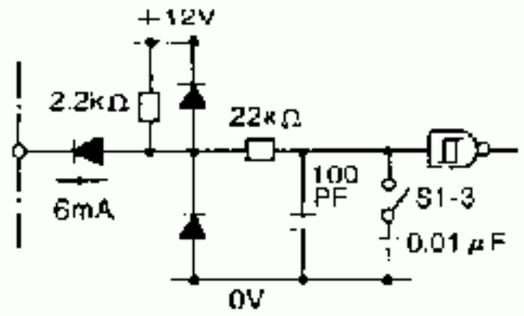
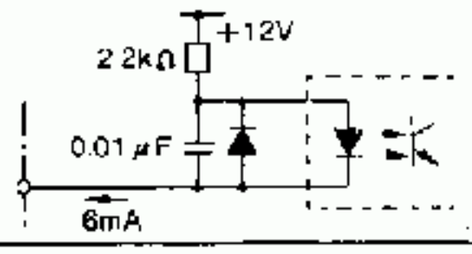
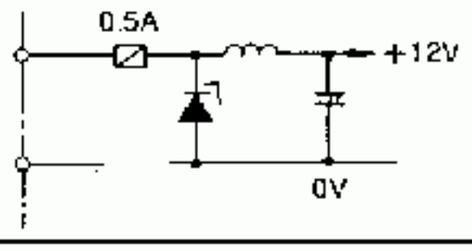
Table 2. 6 Outline of Input Signals

Name	Description
Phase A Pulse Phase B Pulse (Sign)	The pulses input to phase A pulse terminal and to phase B (sign) terminal are counted as the current value by the counter. The counting modes may be selected in the two-phase mode or the single-phase-with-sign mode. Counting may also be selected in the single- or double-counting mode. These selections are set by the mode setting switches on the left side of the module.
SHIELD	This is the terminal to which the shield of the input pulse cable is to be connected. It is connected to the chassis with the module mounting screws.
COUNT ENABLE/ EXTERNAL RESET	To select COUNT ENABLE or EXTERNAL RESET, the setting switch on the side of the module is used. COUNT ENABLE: When counting, the input pulses are enabled at L level and disabled at H level. EXTERNAL RESET: The current value of the module counter is cleared during L level. Input terminal used as EXTERNAL RESET should be at L level when over 2.4 ms.
ADDITION TEST SUBTRACT TEST	When these terminals are connected to 0 V, one pulse only is counted, if the connection is less than 1 second. If connection remains more than 1 second, counting takes place at approx. 10 pps thereafter. This counting is not related to the input pulses. (accepted even while COUNT ENABLE is H only when ENABLE output coil is ON.)
EXTERNAL POWER SUPPLY	This module requires a +12 VDC external power supply.

Note:

1. The three 0 V terminals, Nos. 4, 7 and 11 of the terminal block, are common inside the module.
2. No connection should be made to No. 6 or No. 8 vacant terminals.
3. The No. 10 shield terminal is connected to the chassis by the module mounting screws. Insure that the module mounting screws are tight during operation.

Table 2. 7 Electrical Specifications of Input Signal

Input Signal	Electrical Specifications	Input Circuit
Phase A Pulse Phase B Pulse (Sign)	Input voltage at H level: +10 V min Input voltage at L level: +1.2 V max Max. input voltage: +29 VDC Input current (flowing from input terminal while input voltage is 0 V) 6.0 mA Response time. With both L→H, and H→L. •10 μs max (40 kpps) •1 ms max (400 pps)	
COUNT ENABLE/ EXTERNAL RESET	Input voltage at H level: +10 V min Input voltage at L level: +1.2 V max Max. input voltage: +29 VDC Input current (flowing from input terminal while input voltage is 0 V): 6.0 mA Response time. With both L→H, and H→L. •10 μs max (high speed) •1 ms max (low speed)	
ADDITION TEST/ SUBTRACT TEST	ON requirement: Closed circuit OFF requirement: Open circuit Input current (flowing from input terminal while input circuit is closed): 6.0 mA	
EXTERNAL POWER SUPPLY	Power supply voltage: +12 V ±10 % Current consumption: 0.1 A max Fuse: 0.5 A	

2. 5. 1 Input Signal (Cont'd)

Table 2. 8 Timing of Pulse Count

		Addition	Subtraction
Phases A and B	×1	PHASE A PULSE PHASE B PULSE (SIGN)	PHASE A PULSE PHASE B PULSE (SIGN)
	×2	PHASE A PULSE PHASE B PULSE (SIGN)	PHASE A PULSE PHASE B PULSE (SIGN)
Pulse with Sign	×1	PHASE A PULSE "HIGH" PHASE B PULSE (SIGN)	PHASE A PULSE PHASE B "LOW" PULSE (SIGN)
	×2	PHASE A PULSE "HIGH" PHASE B PULSE (SIGN)	PHASE A PULSE PHASE B "LOW" PULSE (SIGN)

Note:
1. Pulse is counted in the timing of arrow mark ↑.
2. In a double pulse count, up to 80kpps is available (Input pulse: 40kpps max).

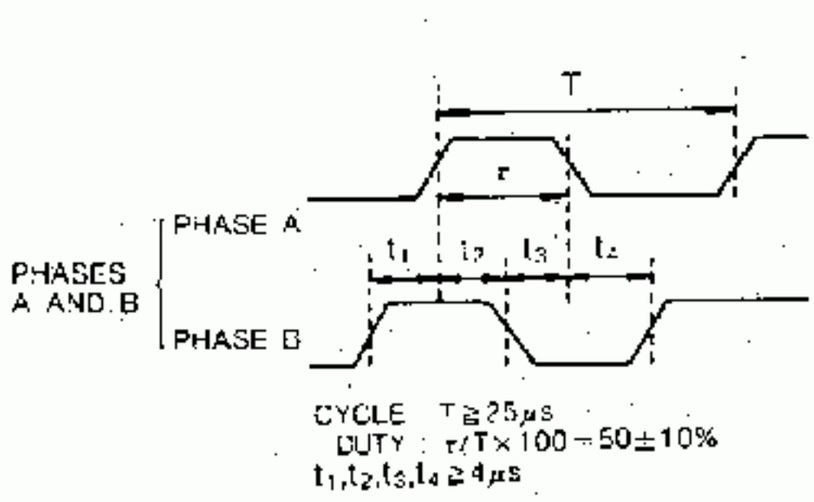


Fig. 2. 4 Input Pulse Waveform

2. 5. 2 Indication Lamp

Fig. 2. 5 shows the position of the indication lamps, and Table 2. 9 gives a brief description of the lamps.

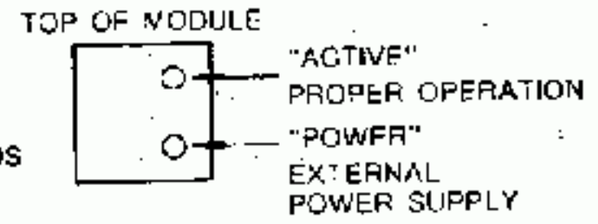


Fig. 2. 5
Layout of Indication Lamps

Table 2. 9 Outline of Indication Lamps

Indication lamp	Description
ACTIVE	This lamp is on while the module is self-diagnosed to be in order, and data exchange with the mainframe is normal
POWER	This lamp is on while +12 V external power supply is on.

2. 6 SETTING SWITCH

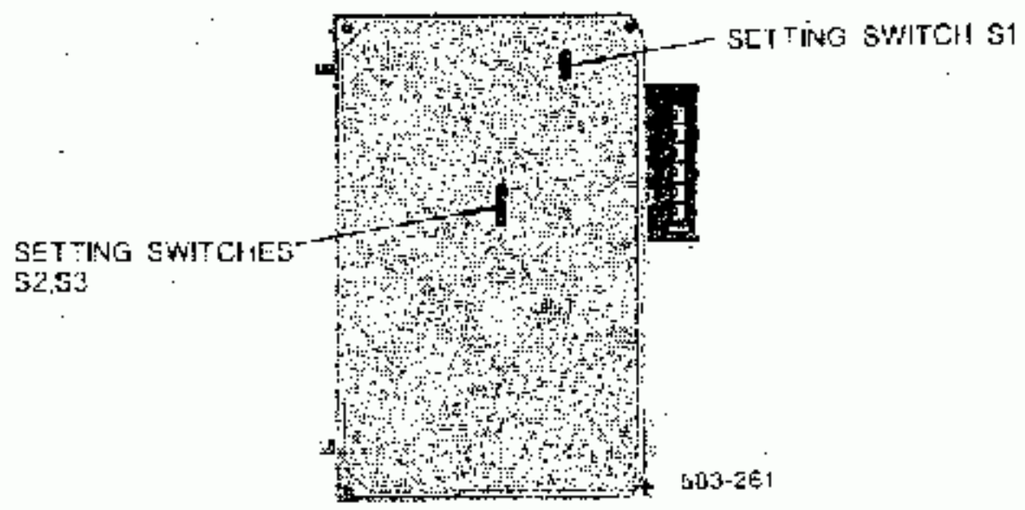


Fig. 2. 6 Location of Setting Switches S1, S2 and S3

2. 6. 1 Function of Setting Switch S1 (Response Frequency Selection)

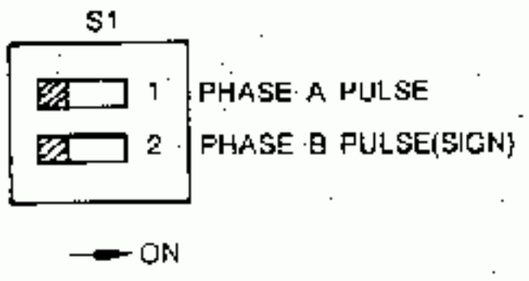


Table 2. 10 Function of Setting Switch S1

Setting Switch	OFF	ON
S 1-1	40 kpps	400 pps
S 1-2	40 kpps	400 pps

Note: Be sure S1-1 and S1-2 are set equally.

2.6.2 Function of Setting Switch S2
(Input Pulse Selection)

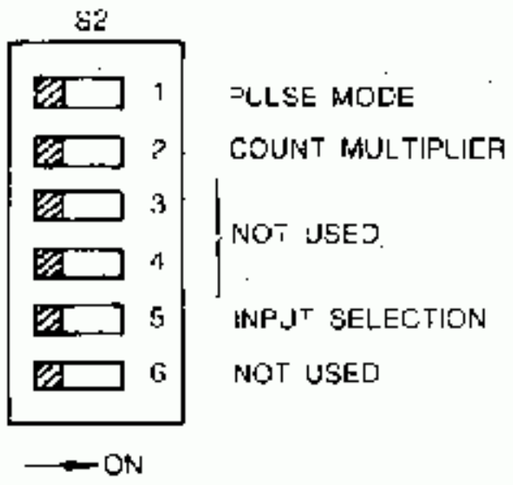


Table 2.11 Function of Setting Switch S2

Setting Switch	OFF	ON
S 2-1	Phases A and B	Pulse with sign
S 2-2	×1	×2
S 2-5	COUNT ENABLE	EXTERNAL RESET

2.6.3 Function of Setting Switch S3
(Setting Mode Selection)

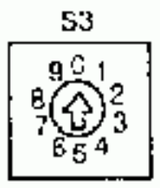


Table 2.12 Function of Setting Switch S3

Setting Switch	Setting Mode
S 3-0	Decimal 6 digits for R841
S 3-1 to S 3-4	Not used.
S 3-5	Decimal 8 digits for U84 , U84J and 584
S 3-6 to S 3-9	Not used.

Note: The setting mode is read in by the module only during the power up process.

IMPORTANT

When the module is delivered, S1 and S2 for all the setting switches are OFF, and S3 is S3-0.

2.7 ELEMENT LAYOUT OF FRONT PANEL

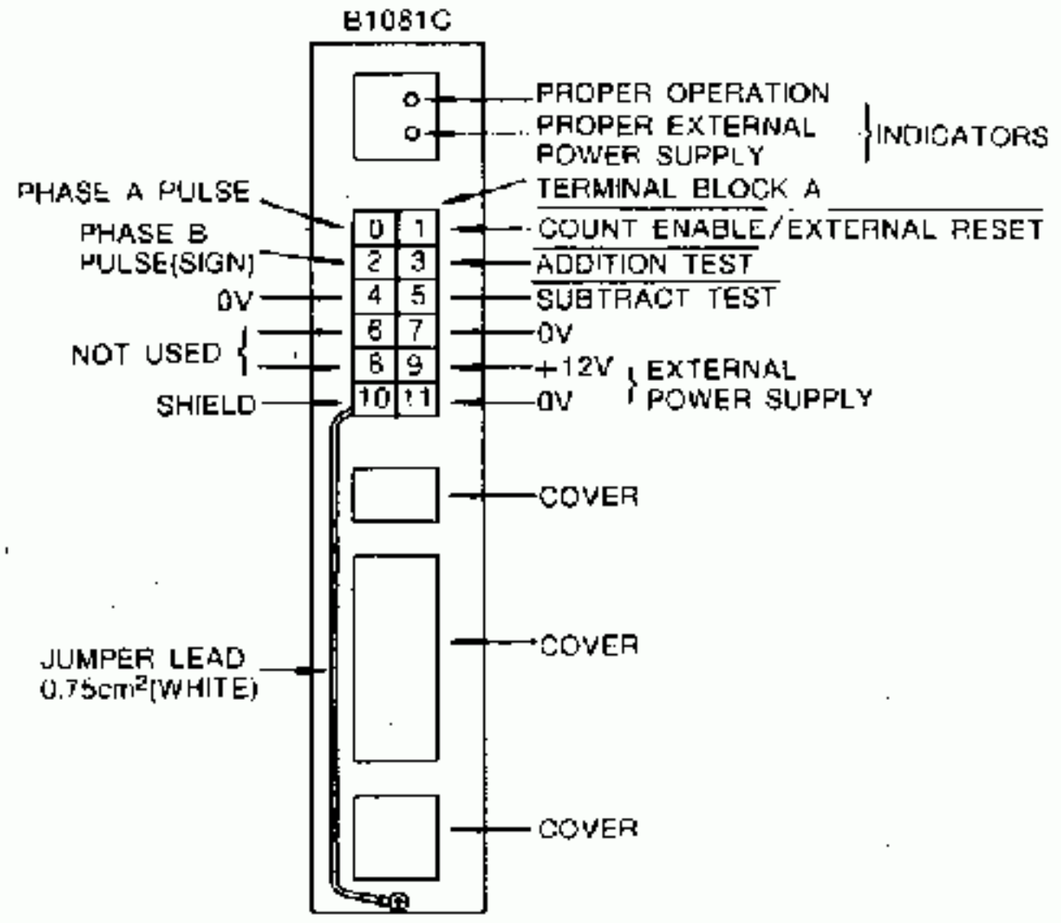


Fig. 2.7 Element Layout on Front Panel of B1081C

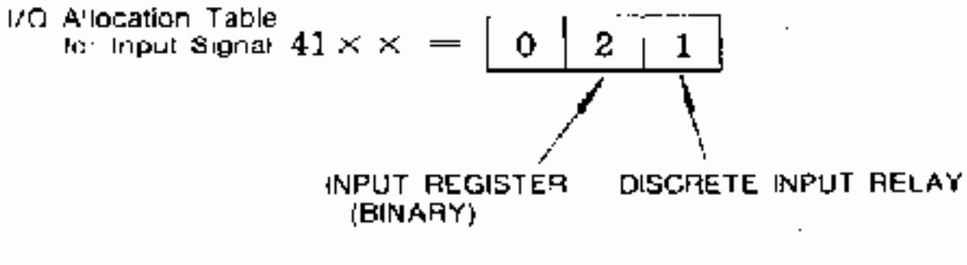
2.8 INPUT/OUTPUT ALLOCATION

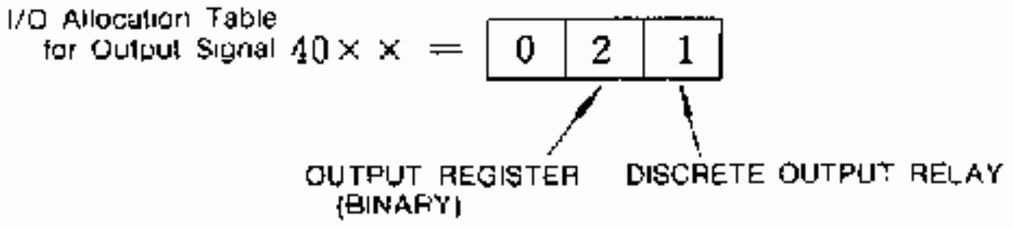
2.8.1 R84H I/O Allocation

Similar to other I/O modules, B1081C requires I/O allocation to exchange signals with the R84H. For details of the I/O allocation, refer to Memocon-SC R84H DESIGNER'S REFERENCE MANUAL: SIE-C815-9.4. B1081C requires the following allocations.

- Discrete input relay: 8
- Input register: 2
- Discrete output coil: 8
- Output register: 2

The I/O allocation for B1081C is as follows:





NOTE

Be sure to specify binary numbers for I/O registers.

2.8.2 U84, U84J I/O Allocation

In the U84 or U84J I/O allocation, B1081C requires the same number of I/O points as those of the R84H.

- Discrete input relay: 8
- Input register: 2
- Discrete output coil: 8
- Output register: 2

Reference number must be specified as well.

Fig. 2.8 shows a sample U84, U84J I/O allocation on CRT screen of P190 programming panel, where B1081C is inserted into slot 1 of rack 2 in U84, U84J channel 1.

CHANNEL : 01 RACK : 2

INPUT

SLOT	DISCRETE REF #	DISCRETE POINTS	REGISTER REF #	REGISTER BCD	REGISTER BINARY
1	10049	8	30018	INHIBIT	2
2	.....	INHIBIT	.....	INHIBIT	INHIBIT
3	.....	INHIBIT	.....	INHIBIT	INHIBIT

CHANNEL : 01 RACK : 2

OUTPUT

SLOT	DISCRETE REF #	DISCRETE POINTS	REGISTER REF #	REGISTER BCD	REGISTER BINARY
1	00049	8	40017	INHIBIT	2
2	.....	INHIBIT	.....	INHIBIT	INHIBIT
3	.....	INHIBIT	.....	INHIBIT	INHIBIT

Fig. 2.8 Sample U84, U84J I/O Allocation

2.8.3 584 I/O Allocation

Where 1000 series I/O module is connected to Memocon-SC584, an I/O adapter, Type DISCT-J1040 is required. I/O allocation must be set for both the 584 and the adapter. For the adapter I/O allocation, refer to "Memocon-SC584 1000 SERIES I/O ADAPTER" (SIE-C815-7.80).

B1081C requires the following number of I/O points.

- Discrete input relay: 16
- Input register: 2
- Discrete output coil: 16
- Output register: 2

A sample 584 I/O allocation is shown in Fig. 2.9, using CRT screen of P190 programming panel. Fig. 2.10 lists an example of I/O allocation conversion table for the J1040 adapter, where B1081C is inserted into slot 1 of the J1040.

CHANNEL : 01

INPUT SLOT	INPUT REF	INPUT TYPE	OUTPUT SLOT	OUTPUT REF	OUTPUT TYPE
1	10001	DISCRETE	1	00001	DISCRETE
2	30001	BIN REG	2	40001	BIN REG
3	30002	BIN REG	3	40002	BIN REG
4	.....	INHIBIT	4	.....	INHIBIT
5	.....	INHIBIT	5	.....	INHIBIT
6	.....	INHIBIT	6	.....	INHIBIT
7	.....	INHIBIT	7	.....	INHIBIT
8	.....	INHIBIT	8	.....	INHIBIT

Note: Be sure to specify binary numbers for I/O registers.

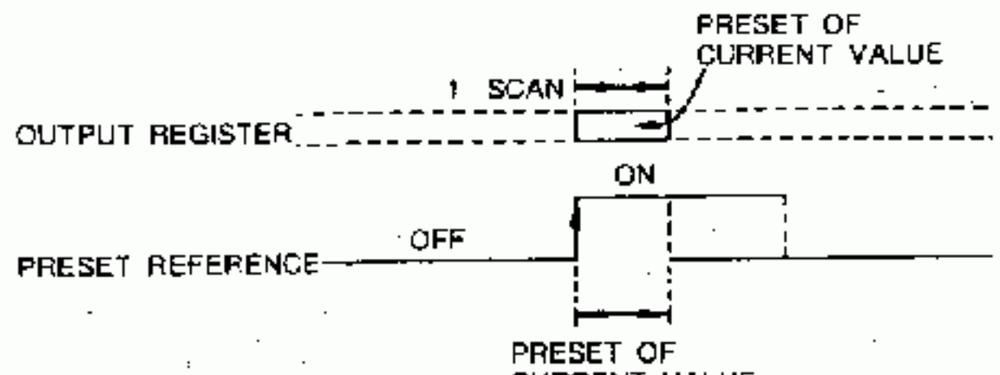
Fig. 2.9 Sample 584 I/O Allocation

	Input				Output			
	584		1000 Series I/O		584		1000 Series I/O	
	SLOT	Input	R/D	Slot	SLOT	Output	R/D	SLOT
Odd Channel	1	10001	D	01	1	00001	D	01
	2	30001	R	01	2	40001	R	01
	3	30002	R	01	3	40002	R	01
	4	INHIBIT	—	—	4	INHIBIT	—	—
	5	INHIBIT	—	—	5	INHIBIT	—	—
	6	INHIBIT	—	—	6	INHIBIT	—	—
	7	INHIBIT		—	7	INHIBIT	—	—
	8	INHIBIT	—	—	8	INHIBIT	—	—

Fig. 2.10 Example of I/O Allocation Conversion Table for J1040 Adapter

2.9 PRESETTING

Fig. 2.11 shows the presetting of B1081C, and Fig. 2.12 shows a sample preset circuit.



Note:
1. PRESET REFERENCE is always effective.
2. Keep PRESET REFERENCE ON for 1 scan or longer.
3. In the scan prior to turning PRESET REFERENCE on, or in which PRESET REFERENCE is turned on, the corresponding output registers must contain the current preset counts.
4. To preset again, the PRESET REFERENCE must be turned off, and then turned on again.
5. Unless presetting is made in the module, the current value of counter can always be monitored by the input register. However, during presetting, the input register contents are uncertain.

Fig. 2.11 Presetting Operation

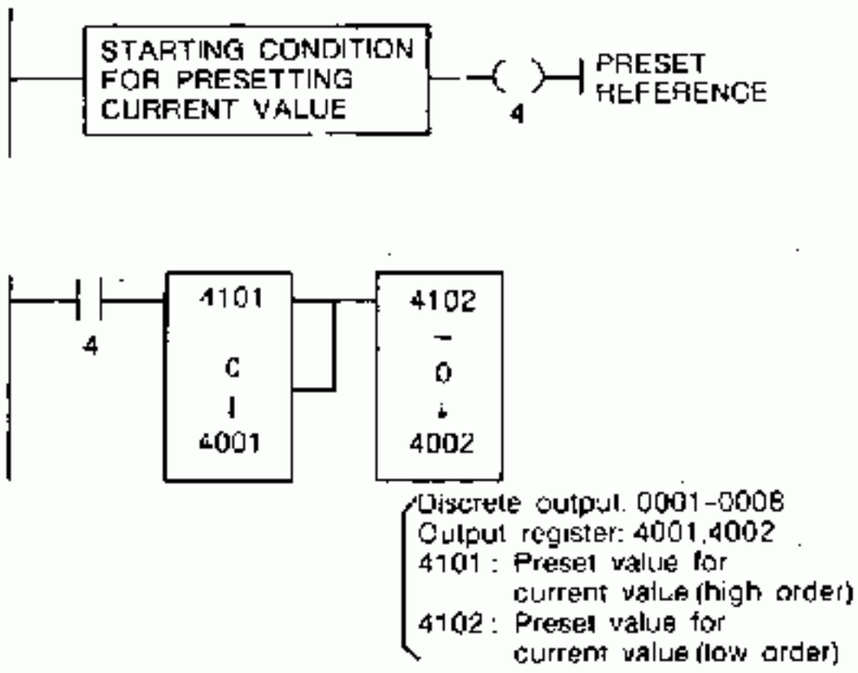


Fig. 2.12 Example of Preset Circuit (R84H)

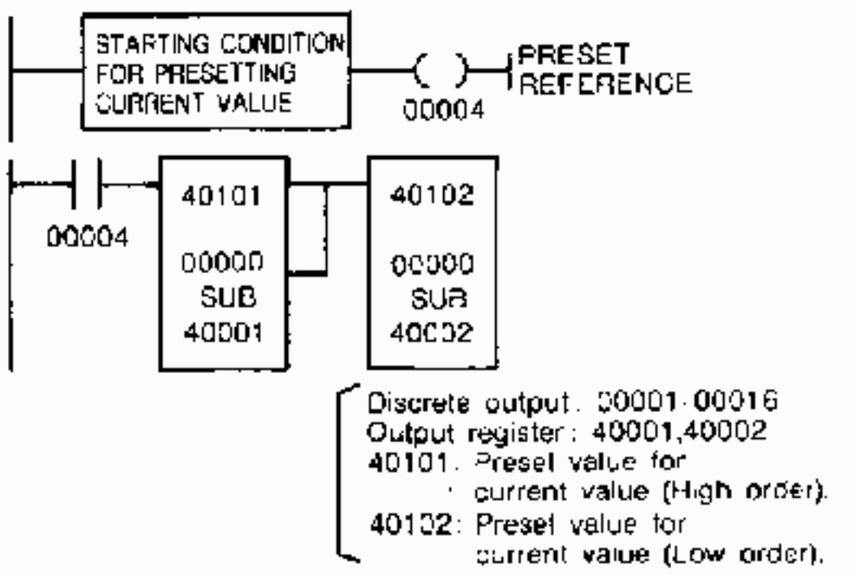


Fig. 2.13 Example of Preset Circuit (U84, U84J, 584)

2.10 CARRY AND BORROW

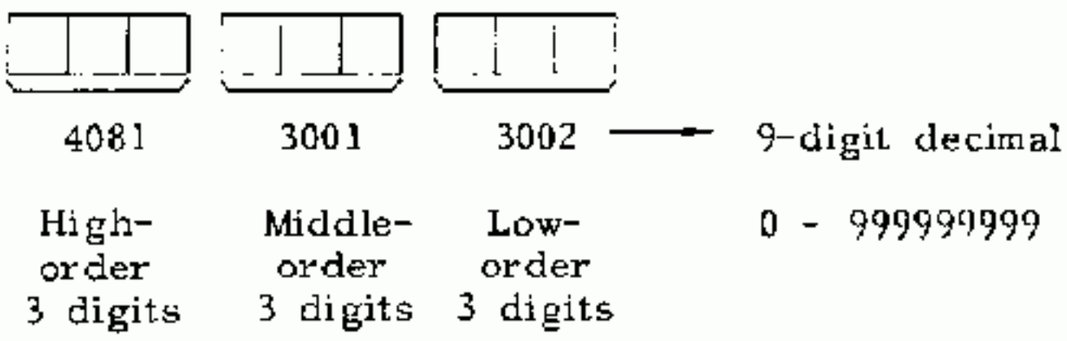
When more than 6-digit or 8-digit places are required for counting, digits can be carried and/or borrowed from the module. Figs. 2.14 and 2.15 show examples of ladder diagrams.

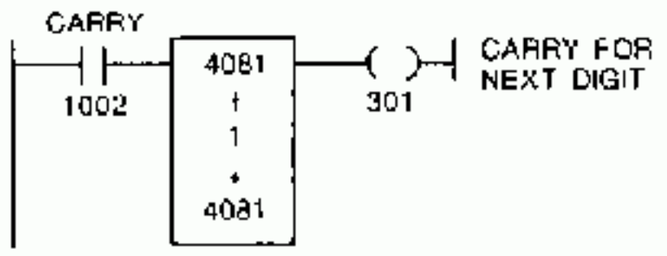
Discrete input: 1001 - 1008

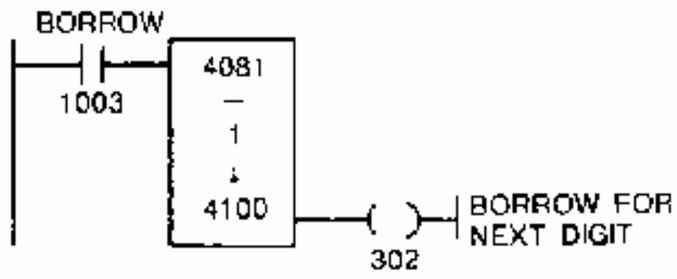
Register input: 3001, 3002

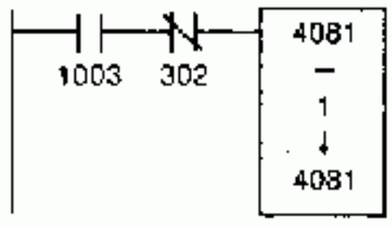
4081: High-order digit register

4100: Work register









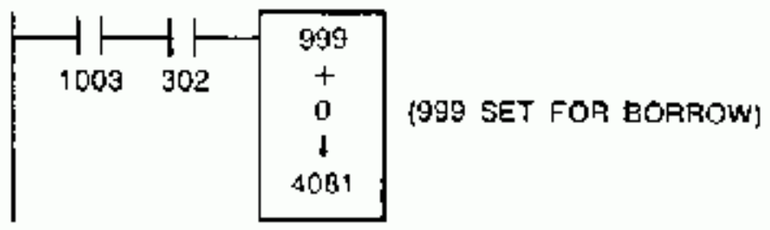


Fig. 2.14 Example of Ladder Diagram for Carry and Borrow (R84H)

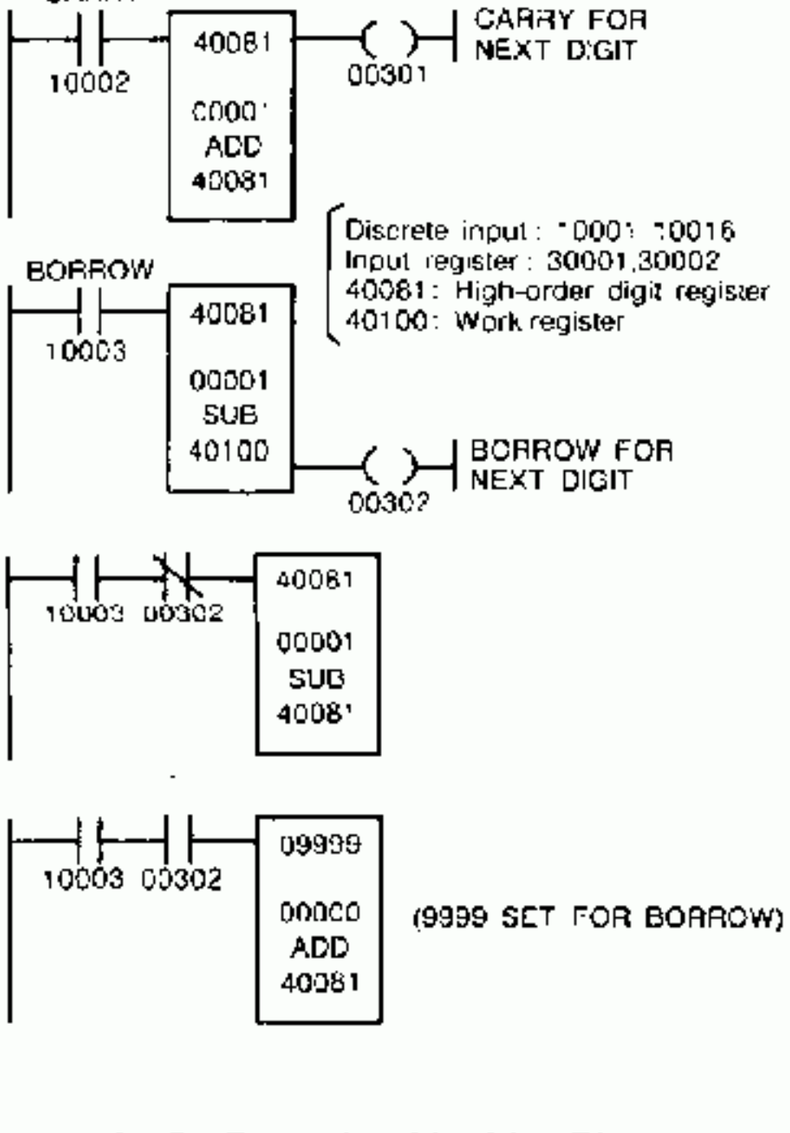


Fig. 2.15 Example of Ladder Diagram for Carry and Borrow (U84, U84J, 584)

2.11 SELF DIAGNOSIS

2.11.1 Diagnostic Contents

(1) Power up diagnosis

- ROM total check
- RAM check

(2) Always

- ROM total check
- WDT check
- Bus interface time out error

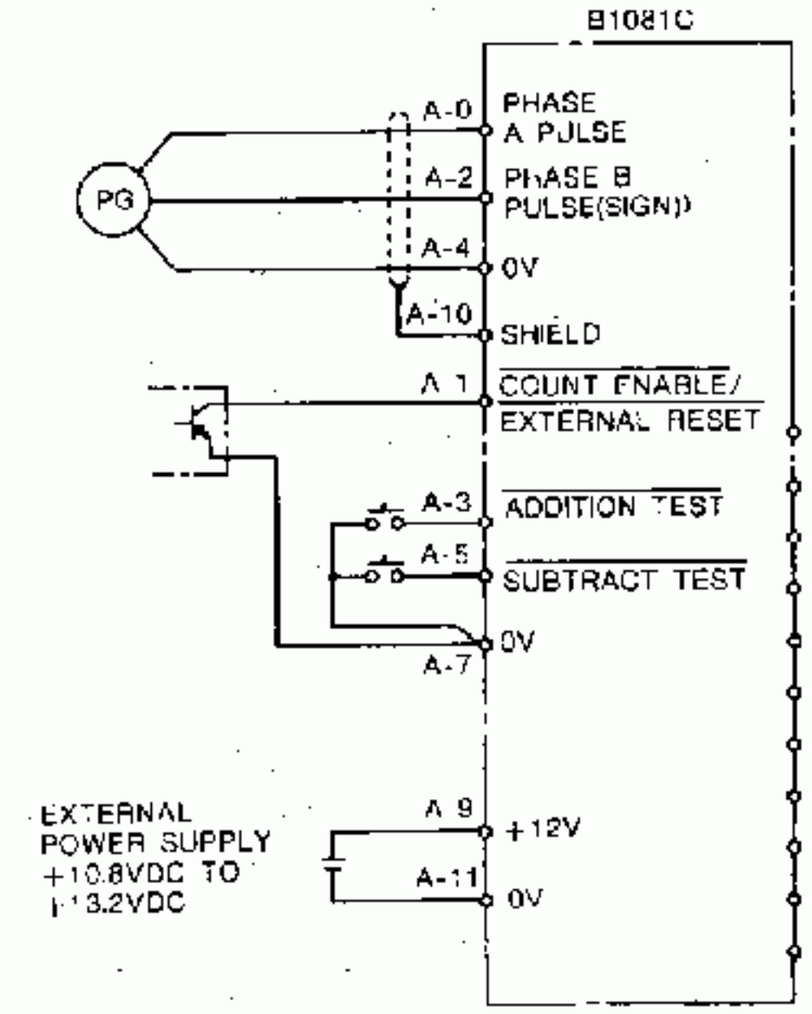
2.11.2 Procedure under Fault State

Table 2.13 Procedure under Fault State

Error	Hardware errors •Those detected by self diagnosis: [ROM total check RAM check WDT check] •Program running away through hardware error.	Bus interface time out error •Mainframe failure •Mainframe stopped by programming panel (PP).
ACTIVE Lamp	Off	Off
READY	Off	On (but no access to mainframe)
Bus Interface	No module state as viewed from mainframe.	Disconnected
Restoring Method	If detected by self diagnosis: Initial start by MODULE RESET. If hardware error occurs again replace module. If program runs away, turn on and off power supply for initial start. If hardware error occurs again, replace module.	If mainframe fails, turn mainframe power on and off to initial start. When stopped by PP, start mainframe to restore.

Note: When the CPU is memory-cleared state, READY input relay may be OFF because of rapid scanning time. This is not error. Store several ladder circuits to obtaine ON state of the relay.

2.12 EXTERNAL CONNECTION



Note:
1. To connect to the PG, be sure to use shielded cable, and connect the shield to the SHIELD terminal. In principle, the length of PG cable must not exceed 30m for 40kpps.
2. When the COUNT ENABLE/EXTERNAL RESET terminal is not used, select COUNT ENABLE by the setting switch S2-5 and connect it to 0V.

Fig. 2.16 External Connection Diagram

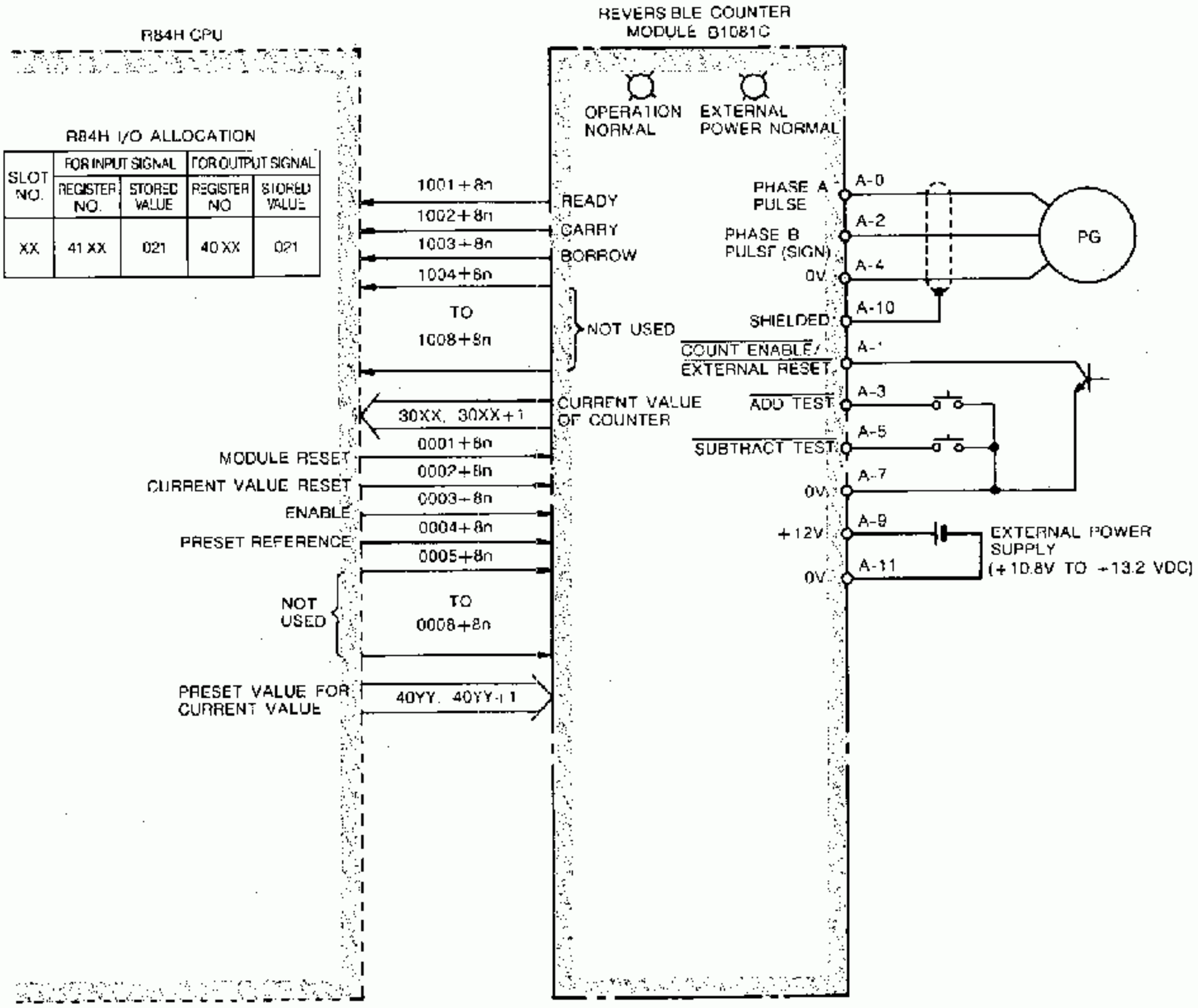


Fig. 2.17 Connection of Reversible Counter Module (B1081C) and R84H

3. PRESET COUNTER (TYPE JAMSC-B1082C)

3.1 SUMMARY

Fig. 3.1 shows the exterior view of B1082C. B1082C is mounted on the mounting base of 1000 series I/O. It is the same size as one normal discrete I/O module (1 span) of the 1000 series I/O, and can be inserted in any of the slots in the mounting base.

The external wiring terminal blocks and the indication lamps are located on the front face of the module. Each external wiring terminal block has 12 pins, and up to two 1.25mm^2 wires can be connected to each pin. The terminal block is attached to the module with two screws, so that when the module is to be replaced, only these two screws need be removed without the individual wires being disconnected.

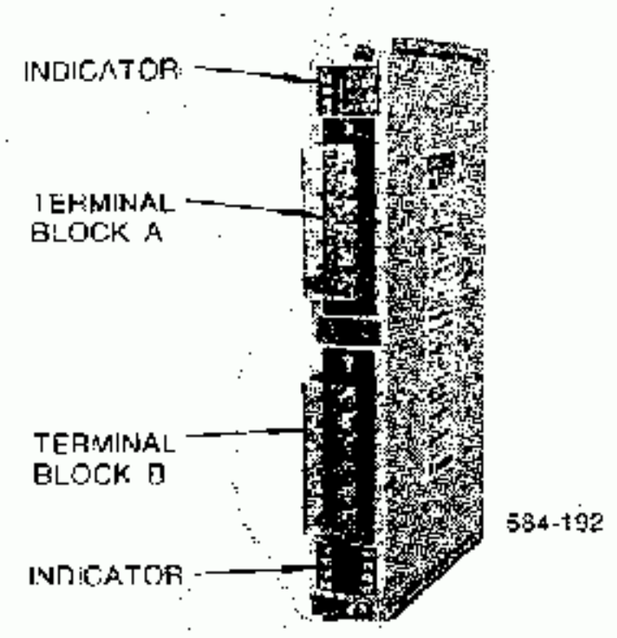


Fig. 3.1 Exterior View of B1082C

The setting switches on the left side of the module are for selection of the pulse modes. Fig. 3.2 shows the block diagram of B1082C.

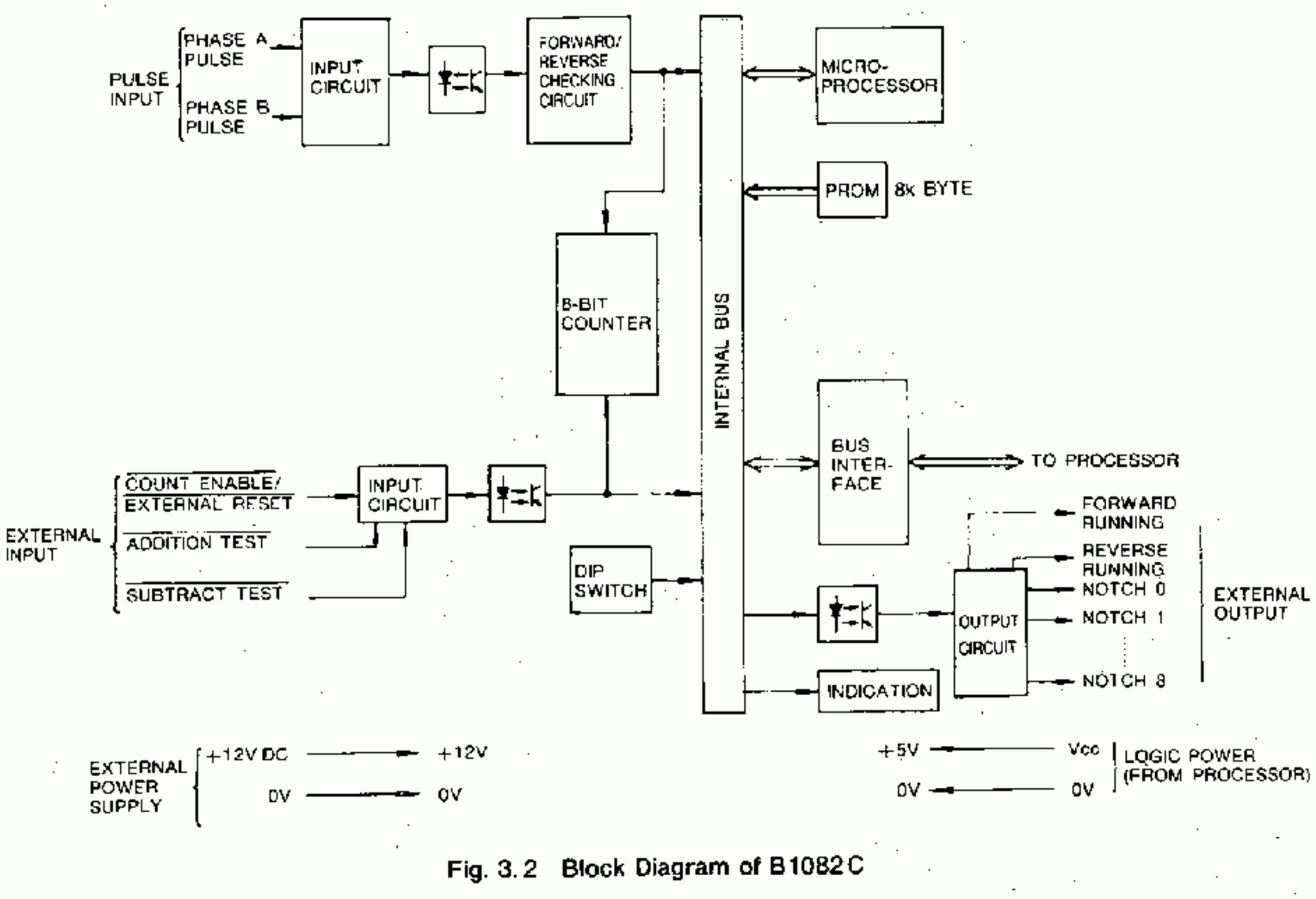


Fig. 3.2 Block Diagram of B1082C

As the input pulses, either two-phase or single-phase-with-sign pulses can be used, and as the pulse count scaling, single- or double-counting mode can be selected, with the setting switch. For counting low speed pulses with high noise content, low input pulse rates (400 pps) can be selected with the setting switch.

In addition, external signals $\overline{\text{COUNT ENABLE}}$ and $\overline{\text{ADDITION TEST}}$ and $\overline{\text{SUBTRACT TEST}}$ signals can be accomodated. With the latter two, the current module values can be increased or decreased without inputting external pulses, for convenient checking during test run or trouble-shooting.

With B1082C, external output signals $\overline{\text{FORWARD}}$, $\overline{\text{REVERSE}}$, $\overline{\text{NOTCH 0}}$, through $\overline{\text{NOTCH 8}}$ are available. $\overline{\text{FORWARD}}$ and $\overline{\text{REVERSE}}$ are the output signals from the mainframe as received.

$\overline{\text{NOTCH 0}}$ through $\overline{\text{NOTCH 8}}$ are output by the module on the basis of the comparison between the current value of counter and the setting for notch points N1 through N8, given in advance by the mainframe. See Fig. 3.3 .

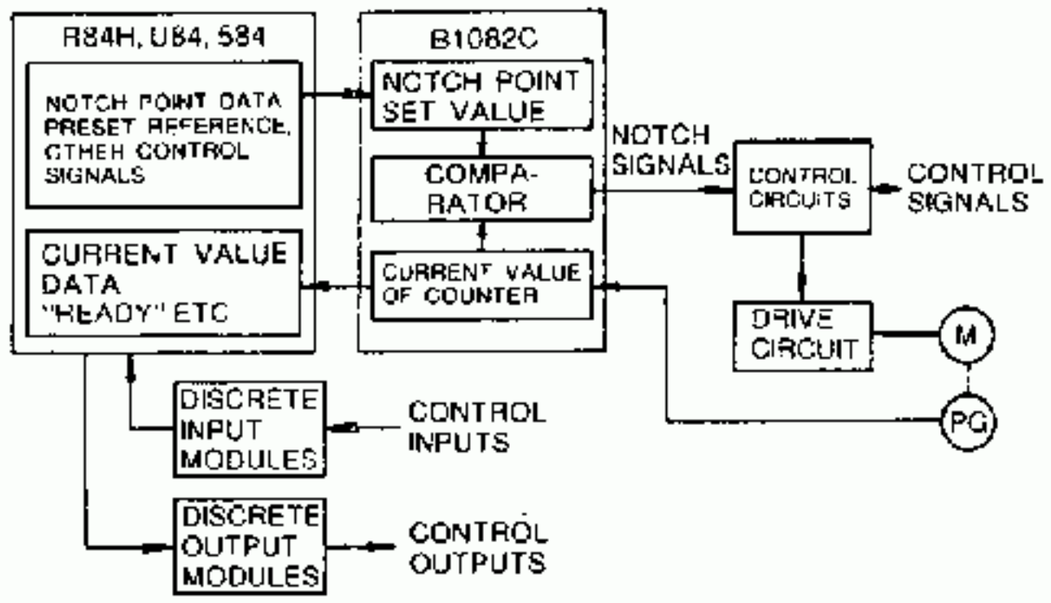


Fig. 3.3 Conceptual Diagram of Notch Control

3.2 SPECIFICATIONS

Table 3.1 Specifications

Item	Specifications
Name	Preset counter module
Type	JAMSC-B1082C
Ambient Temperature	0 to + 55 °C
Storage Temperature	−20 °C to +85 °C
Humidity	5 % to 95 % RH (non-condensing)
Vibration Resistance	In compliance with JIS* C0911
Shock Resistance	10 G max
Environmental Condition	Free from explosive, inflammable and corrosive gas
Dielectric Strength	500 VDC
Number of Circuits	one circuit/module
Mainframes	*Memocon-SC* R84H, U84, U84J, 584
Number of Digits	decimal 6 digits for R84H and 8 digits for U84, U84J 584
Max. Counting Speed	40 kpps or 400 pps (swilchable)
Input Pulse Mode	2-phase or single-phase-with-sign (switchable)
Pulse Count Multiplier	×1 or ×2 (switchable)
System Response Time	5 ms max (overall response time from pulse input terminal to notch output terminal)
Heating Value	10 W max
External Power Supply	+12 VDC ±10 %, 0.1 A max
Dimensions in mm	34.5 (W) × 250 (H) × 199 (D)
Approx. Weight	0.8 kg

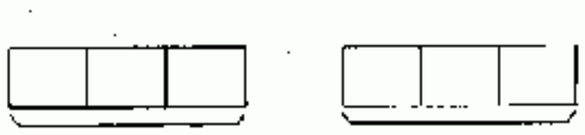
*Japanese Industrial Standard

3.3 INTERNAL INTERFACE (SIGNAL COMMUNICATION WITH R84H)

3.3.1 Module to R84H

(1) Current Value of Counter

While the CURRENT VALUE/NOTCH POINT of the output coil is off, the current value of counter enters two successive input registers (30××, 30×× + 1) in 6-digit decimal. The input registers used are determined by the R84H I/O allocation.



High-order 3 digits	Low-order 3 digits	6-digit decimal
30××	30×× + 1	0 - 999999

(2) Notch Point Set Value

While CURRENT VALUE/NOTCH POINT of the output coil is on, the notch point set value is put in the same input registers as those for the current value of counter in 6-digit decimal. The data format is the same as for the current value of counter.

(3) Control Signal

Table 3.2 shows the outline of the control signals (discrete input relay).

3.3.2 R84H to Module

(1) Presetting Current Value

To preset the current value (6-digit decimal) from the R84H to the module, two consecutive output registers (40××, 40×× + 1) are used. The output registers to be used are determined by the R84H I/O allocation.

High-order 3 digits	Low-order 3 digits	6-digit decimal
40××	40×× + 1	0 - 999999

Table 3.2 Control Signal (Discrete Input Relay) Outline

Input Relay Signal	Name	Description
1001 − 16n	READY	Module self-diagnostic result. If normal, it is ON, and if not normal, OFF. OFF for approx 0.5 s at power ON or module reset
1002 + 16n	CARRY	When the current value of counter exceeds 999999 and becomes 000000, turns on for one scan.
1003 + 16n	BORROW	When the current value of counter becomes smaller than 000000 (negative), and becomes 999999, turns on for one scan only.
1004 + 16n	ERROR	Turns on when the number of scans for which PRESET REFERENCE is ON is shorter than the number of scans determined by the setting mode.
1005 + 16n	Not usec.	
1006 + 16n		
1007 + 16n		
1008 − 16n	Notch 0	Indicates which notch is output currently from module. The output notch is turned ON.
1009 · 16n	Notch 1	
1010 + 16n	Notch 2	
1011 + 16n	Notch 3	
1012 + 16n	Notch 4	
1013 + 16n	Notch 5	
1014 + 16n	Notch 6	
1015 + 16n	Notch 7	
1016 + 16n	Notch 8	

Note:
1. n = 0 to 15.
2. Input relays of 1005 + 16n to 1007 + 16n cannot be used for other applications.

(2) Notch Point Setting Value

For the notch point setting value, 1 to 4 sets of two consecutive output registers, partly shared in common with the current value presetting output registers, are used. The output registers to be used are determined by the module setting mode select switch and the I/O allocation of the R84H. The data format is the same as that for current value presetting.

(3) Control Signal

Table 3.3 shows the outline of the control signal (discrete output coil).

Table 3.3 Control Signal (Discrete Output Coil) Outline

<table>
<tr><th>Output Coil Number</th><th>Name</th><th>Description</th></tr>
<tr><td>0001+16n</td><td>MODULE RESET</td><td>When MODULE RESET changes from OFF to ON, the module starts the same power up process as that for the initial power switching on, and initializes itself. Possible in 1-scan ON. Always effective.</td></tr>
<tr><td>0002+16n</td><td>CURRENT VALUE RESET</td><td>While CURRENT VALUE RESET is ON, the current value of module counter is kept cleared. Possible in 1-scan ON. Always effective.</td></tr>
<tr><td>0003+16n</td><td>ENABLE</td><td>While ENABLE is ON.
•FORWARD and REVERSE notch outputs can be output.
•Counting of current value is possible.
•Pulse input can be accepted.
While ENABLE is OFF, these functions are disabled.</td></tr>
<tr><td>0004+16n</td><td>PRESET REFERENCE</td><td>When PRESET REFERENCE is turned ON, the $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT coil presets either the current value or the notch point set value. Always effective.</td></tr>
<tr><td>0005+16n</td><td>$\overline{\text{CURRENT VALUE}}$ / NOTCH POINT</td><td>•Presetting:
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is OFF, current value is preset.
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is ON, notch point set value is preset.
•Monitoring (when presetting is not performed):
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is OFF, current value of counter is monitored.
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is ON, notch point set value is monitored</td></tr>
<tr><td>0006+16n</td><td>Notch No. 0</td><td rowspan="4">Only when $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is ON (monitoring notch point set value), these signals are valid, and specify the notch No. to be monitored.
<table>
<tr><th>Notch No. 0</th><th>Notch No. 1</th><th>Notch No. 2</th><th>Notch No. to be Monitored</th></tr>
<tr><td>OFF</td><td>OFF</td><td>OFF</td><td>N 1</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF</td><td>N 2</td></tr>
<tr><td>OFF</td><td>ON</td><td>OFF</td><td>N 3</td></tr>
<tr><td>ON</td><td>ON</td><td>OFF</td><td>N 4</td></tr>
<tr><td>OFF</td><td>OFF</td><td>ON</td><td>N 5</td></tr>
<tr><td>ON</td><td>OFF</td><td>ON</td><td>N 6</td></tr>
<tr><td>OFF</td><td>ON</td><td>ON</td><td>N 7</td></tr>
<tr><td>ON</td><td>ON</td><td>ON</td><td>N 8</td></tr>
</table></td></tr>
<tr><td>0007+16n</td><td>Notch No. 1</td></tr>
<tr><td>0008+16n</td><td>Notch No. 2</td></tr>
<tr><td>0009+16n</td><td>FORWARD</td><td rowspan="2">These FORWARD and REVERSE coils are directly output as module output signals for FORWARD and REVERSE
[ON: output L level (output transistor ON)
OFF: output H level (output transistor OFF)]
ENABLE: if ON, outputting is possible</td></tr>
<tr><td>0010+16n</td><td>REVERSE</td></tr>
<tr><td>0011+16n</td><td>Forced Notch Output 0</td><td rowspan="6">Regardless of the module notch output No., when any of the forced notch outputs is turned ON, the existing notch output is neglected, and the forced notch output is output. When the forced notch output is turned off, the previous notch output is restored. Multiple outputs are possible. When ENABLE is ON, output is possible.</td></tr>
<tr><td>0012+16n</td><td>Forced Notch Output 1</td></tr>
<tr><td>0013+16n</td><td>Forced Notch Output 2</td></tr>
<tr><td>0014+16n</td><td>Forced Notch Output 3</td></tr>
<tr><td>0015+16n</td><td>Forced Notch Output 8</td></tr>
<tr><td>0016+16n</td><td>Forced Notch Output 4</td></tr>
</table>

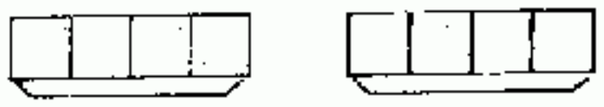
Note: n=0 to 15.

3.4 INTERNAL INTERFACE (SIGNAL COMMUNICATION WITH U84, U84J, 584)

3.4.1 Module to U84, U84J, 584

(1) Current Value of Counter

While the $\overline{\text{CURRENT VALUE}}$/NOTCH POINT of the output coil is off, the current value of counter enters two successive input registers (3××××, 3×××× + 1) in 8-digit decimal. The input registers used are determined by the U84, the U84J or the 584 I/O allocation.



High-order 4 digits	Low-order 4 digits	8-digit decimal
3××××	3 ×××× + 1	0 – 99999999

(2) Control Signal

Table 3.4 shows the outline of the control signals (discrete input relay).

Table 3.4 Control Signal (Discrete Input Relay) Outline

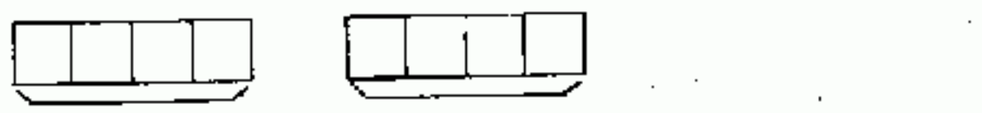
Input Relay Signal	Name	Description
10001+16n	READY	Module self-diagnostic result. If normal, it is ON, and if not normal, OFF. OFF for approx 0.5 s at power ON or module reset.
10002+16n	CARRY	When the current value of counter exceeds 99999999 and becomes 00000000, turns on for one scan.
10003+16n	BORROW	When the current value of counter becomes smaller than 00000000 (negative), and becomes 99999999, turns on for one scan only.
10004+16n	ERROR	Turns on when the number of scans for which PRESET REFERENCE is ON is shorter than the number of scans determined by the setting mode.
10005+16n		Not used.
10006+16n		
10007+16n		
10008+16n	Notch 0	Indicates which notch is output currently from module. The output notch is turned ON.
10009+16n	Notch 1	
10010+16n	Notch 2	
10011+16n	Notch 3	
10012+16n	Notch 4	
10013+16n	Notch 5	
10014+16n	Notch 6	
10015+16n	Notch 7	
10016+16n	Notch 8	

Note:
1. n=0, 1, 2·····
2. Input relay of 10005 +16n to 10007 +16n cannot be used for other applications.

3.4.2 U84, U84J, 584 to Module

(1) Presetting Current Value

To preset the current value (8-digit decimal) from the U84, the U84J or the 584 to the module, two consecutive output registers (4××××, 4×××× + 1) are used. The output registers to be used are determined by the U84, the U84J or the 584 I/O allocation.



High-order 4 digits	Low-order 4 digits	8-digit decimal
4××××	4 ×××× + 1	0 – 99999999

(2) Notch Point Setting Value

For the notch point setting value, 1 to 4 sets of two consecutive output registers, partly shared in common with the current value presetting output registers, are used. The output registers to be used are determined by the module setting mode select switch and the I/O allocation of the U84, the U84J or the 584. The data format is the same as that for current value presetting.

(3) Control Signal

Table 3.5 shows the outline of the control signal (discrete output coil).

Table 3.5 Control Signal (Discrete Output Coil) Outline

<table>
<tr><th>Output Coil Number</th><th>Name</th><th>Description</th></tr>
<tr><td>00001+16n</td><td>MODULE RESET</td><td>When MODULE RESET changes from OFF to ON, the module starts the same power up process as that for the initial power switching on, and initializes itself. Possible in 1-scan ON. Always effective.</td></tr>
<tr><td>00002+16n</td><td>CURRENT VALUE RESET</td><td>While CURRENT VALUE RESET is ON, the current value of module counter is kept cleared. Possible in 1-scan ON. Always effective.</td></tr>
<tr><td>00003+16n</td><td>ENABLE</td><td>While ENABLE is ON:
•FORWARD and REVERSE notch outputs can be output.
•Counting of current value is possible.
•Pulse input can be accepted
While ENABLE is OFF, these functions are disabled.</td></tr>
<tr><td>00004+16n</td><td>PRESET REFERENCE</td><td>When PRESET REFERENCE is turned ON, the $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT coil presets either the current value or the notch point set value. Always effective.</td></tr>
<tr><td>00005+16n</td><td>$\overline{\text{CURRENT VALUE}}$ / NOTCH POINT</td><td>•Presetting:
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is OFF, current value is preset.
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is ON, notch point set value is preset.
•Monitoring (when presetting is not performed):
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is OFF, current value of counter is monitored.
If $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is ON, notch point set value is monitored.</td></tr>
<tr><td>00006+16n</td><td>MONITOR 0</td><td rowspan="3">Only when $\overline{\text{CURRENT VALUE}}$ / NOTCH POINT is ON (monitoring notch point set value), these signals are valid and specify the notch No. to be monitored.
<table>
<tr><th>MONITOR 0</th><th>MONITOR 1</th><th>MONITOR 2</th><th>Notch No. to be Monitored</th></tr>
<tr><td>OFF</td><td>OFF</td><td>OFF</td><td>N 1</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF</td><td>N 2</td></tr>
<tr><td>OFF</td><td>ON</td><td>OFF</td><td>N 3</td></tr>
<tr><td>ON</td><td>ON</td><td>OFF</td><td>N 4</td></tr>
<tr><td>OFF</td><td>OFF</td><td>ON</td><td>N 5</td></tr>
<tr><td>ON</td><td>OFF</td><td>ON</td><td>N 6</td></tr>
<tr><td>OFF</td><td>ON</td><td>ON</td><td>N 7</td></tr>
<tr><td>ON</td><td>ON</td><td>ON</td><td>N 8</td></tr>
</table></td></tr>
<tr><td>00007+16n</td><td>MONITOR 1</td></tr>
<tr><td>00008+16n</td><td>MONITOR 2</td></tr>
<tr><td>00009+16n</td><td>FORWARD</td><td rowspan="2">These FORWARD and REVERSE coils are directly output as module output signals for FORWARD and REVERSE.
[ON: output L level (output transistor ON)
OFF: output H level (output transistor OFF)]
ENABLE: if ON, outputting is possible.</td></tr>
<tr><td>00010+16n</td><td>REVERSE</td></tr>
<tr><td>00011+16n</td><td>Forced Notch Output 0</td><td rowspan="6">Regardless of the module notch output No., when any of the forced notch outputs is turned ON, the existing notch output is neglected, and the forced notch output is output. When the forced notch output is turned off, the previous notch output is restored. Multiple outputs are possible. When ENABLE is ON, output is possible.</td></tr>
<tr><td>00012+16n</td><td>Forced Notch Output 1</td></tr>
<tr><td>00013+16n</td><td>Forced Notch Output 2</td></tr>
<tr><td>00014+16n</td><td>Forced Notch Output 3</td></tr>
<tr><td>00015+16n</td><td>Forced Notch Output 8</td></tr>
<tr><td>00016+16n</td><td>Forced Notch Output 4</td></tr>
</table>

Note: n=0, 1, 2·····

3.5 EXTERNAL INTERFACE

3.5.1 Input Signals
(Fig. 3.4, Tables 3.6, 3.7, 3.8)

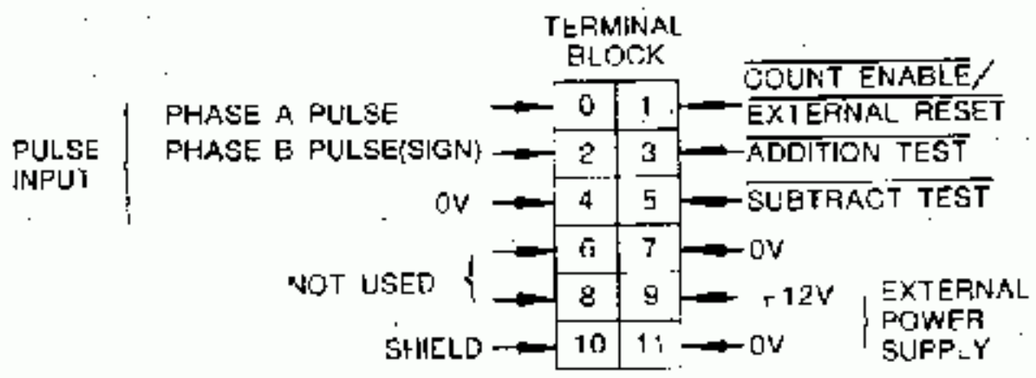


Fig. 3.4 Input Terminal Layout

Table 3.6 Outline of Input Signals

Name	Description
Phase A Pulse Phase B Pulse (Sign)	The pulses input to phase A pulse terminal and to phase B (sign) terminal are counted as the current value by the counter. The counting modes may be selected in the two-phase mode or the single-phase-with-sign mode. Counting may also be selected in the single- or double-counting mode. These selections are set by the mode setting switches on the left side of the module.
SHIELD	This is the terminal to which the shield of the input pulse cable is to be connected. It is connected to the chassis with the module mounting screws.
COUNT ENABLE/ EXTERNAL RESET	To select COUNT ENABLE or EXTERNAL RESET, the setting switch on the side of the module is used. COUNT ENABLE: When counting, the input pulses are enabled at L level and disabled at H level. EXTERNAL RESET: The current value of the module counter is cleared during L level. Input terminal used as EXTERNAL RESET should be at L level when over 2.4 ms.
ADDITION TEST SUBTRACT TEST	When these terminals are connected to 0 V, one pulse only is counted, if the connection is less than 1 second. If connection remains more than 1 second, counting takes place at approx. 10 pps thereafter. This counting is not related to the input pulses. (accepted even while COUNT ENABLE is H only when ENABLE output coil is ON.)
EXTERNAL POWER SUPPLY	This module requires a −12 VDC external power supply.

Note:
1. The three 0 V terminals, Nos. 4, 7 and 11 of the terminal block, are common inside the module.
2. No connection should be made to No. 6 or No. 8 vacant terminals.
3. The No. 10 shield terminal is connected to the chassis by the module mounting screws. Insure that the module mounting screws are tight during operation.

Table 3.7 Electrical Specifications of Input Signal

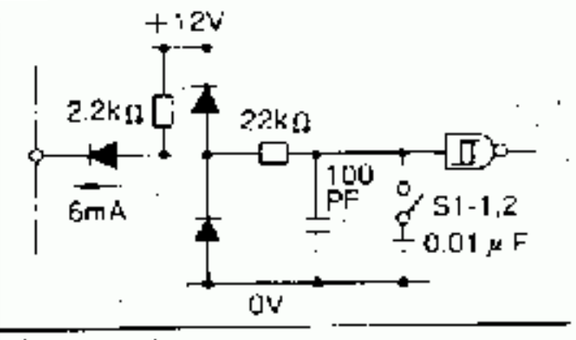
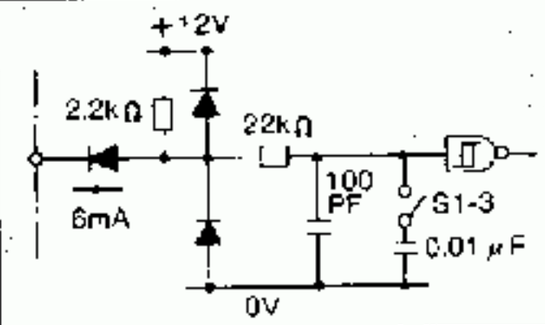
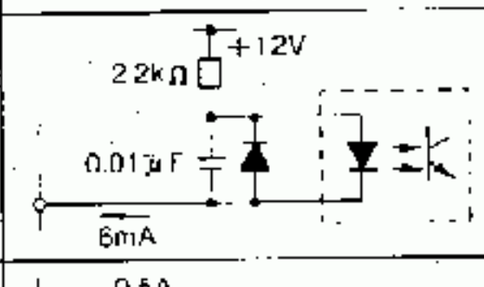
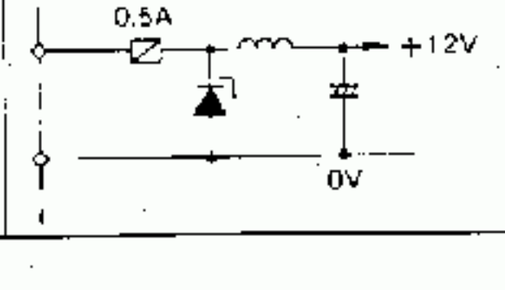
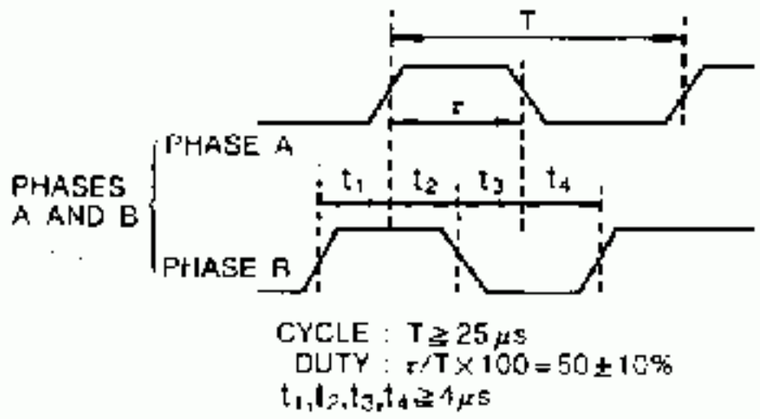
Input Signal	Electrical Specifications	Input Circuit
Phase A Pulse Phase B Pulse (Sign)	Input voltage at H level: +10 V min Input voltage at L level: +1.2 V max Max. input voltage: +29 VDC Input current (flowing from input terminal while input voltage is 0 V): 6.0 mA Response time: With both L→H, and H→L, •10 μs max (40 kpps) •1 ms max (400 pps)	
COUNT ENABLE/ EXTERNAL RESET	Input voltage at H level: +10 V min Input voltage at L level: +1.2 V max Max. input voltage: +29 VDC Input current (flowing from input terminal while input voltage is 0 V): 6.0 mA Response time: With both L→H, and H→L, •10 μs max (high speed) •1 ms max (low speed)	
ADDITION TEST/ SUBTRACT TEST	ON requirement: Closed circuit OFF requirement: Open circuit Input current (flowing from input terminal while input circuit is closed): 6.0 mA	
EXTERNAL POWER SUPPLY	Power supply voltage: 12 V ±10 % Current consumption: 0.1 A max Fuse: 0.5 A	

Table 3.8 Timing of Pulse Count

		Addition	Subtraction
Phases A and B	×1	PHASE A PULSE PHASE B PULSE PHASE PULSE (SIGN)	PHASE A PULSE PHASE B PULSE PHASE PULSE (SIGN)
	×2	PHASE A PULSE PHASE B PULSE PHASE PULSE (SIGN)	PHASE A PULSE PHASE B PULSE PHASE PULSE (SIGN)
Pulse with Sign	×1	PHASE A PULSE "HIGH" PHASE B PULSE (SIGN)	PHASE A PULSE PHASE B PULSE (SIGN) "LOW"
	×2	PHASE A PULSE "HIGH" PHASE B PULSE (SIGN)	PHASE A PULSE PHASE B PULSE (SIGN) "LOW"

Note:
1. Pulse is counted in the timing of arrow mark ↑↓.
2. In a double pulse count, up to 80kpps is available (Input pulse: 40kpps max).



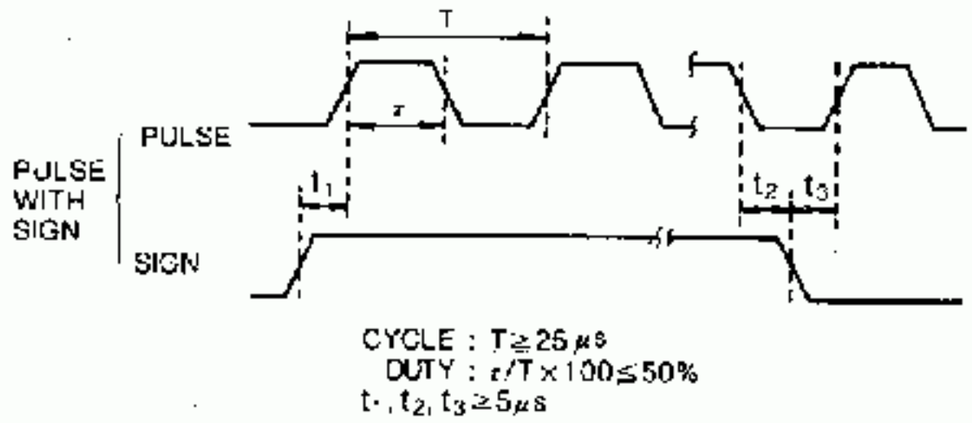


Fig. 3.5 Input Pulse Waveform

3.5.2 Output Signals

(Fig. 3.6, Tables 3.9, 3.10)

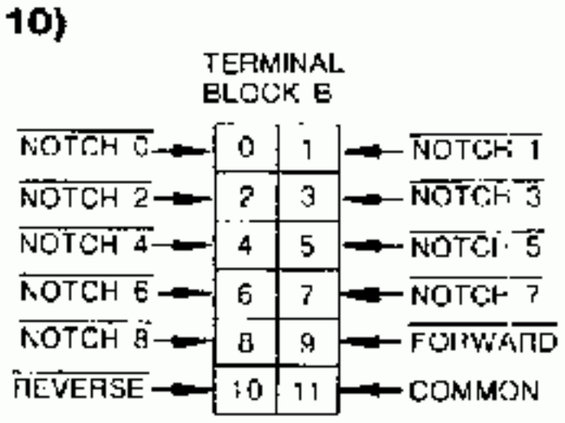


Fig. 3.6 Output Terminal Layout

Table 3.9 Outline of Output Signals

Name	Description
FORWARD REVERSE	The FORWARD and REVERSE signals output from the mainframe are output directly
NOTCH 0 to NOTCH 8	The module outputs these signals on the basis of the comparison between the notch point set value preset in advance by the mainframe and the current value of counter. If a forced notch output is on, it has the priority.

3.5.3 Indication Lamp

Fig. 3.7 shows the layout of the indication lamps, and Table 3.11 gives a brief description.

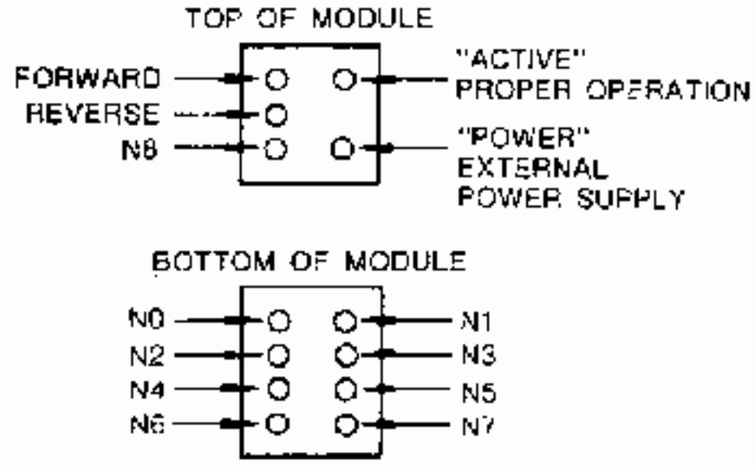
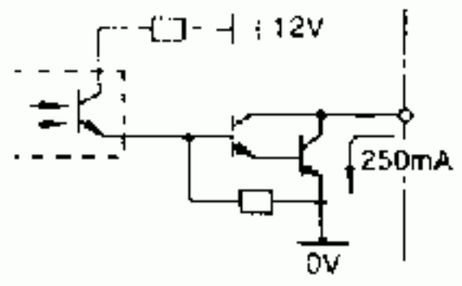


Fig. 3.7 Location of Indication Lamps

Table 3.10 Electrical Specifications of Output Signal

Output Signal	Electrical Specifications		Output Circuit
FORWARD REVERSE	•Open collector output •Negative logic (Effective at L) •Max load voltage: +29 V •Max load current: 250 mA	•ON voltage: 1.0 V max. •Flywheel diode: none •Output protection fuse: none	
NOTCH 0 to NOTCH 8	•Open collector output •Negative logic (Effective at L) •Max load voltage: +29 V •Max load current: 250 mA	•ON voltage: 1.0 V max. •Flywheel diode: none •Output protection fuse: none	

3.5.3 Indication Lamp (Cont'd)

Table 3.11 Outline of Indication Lamps

Indication Lamp	Description
"ACTIVE" Proper Operation	This lamp is on while the module is self-diagnosed to be in order, and data exchange with the main-frame is normal.
"POWER" External Power Supply	This lamp is on while +12 V external power supply is on.
FORWARD REVERSE	These lamps light alternately when a FORWARD or REVERSE signal is output (turning on at L level).
N 0 to N 8	These lamps light when the respective notch signal is output (turning on at L level).

3.6 SETTING SWITCH

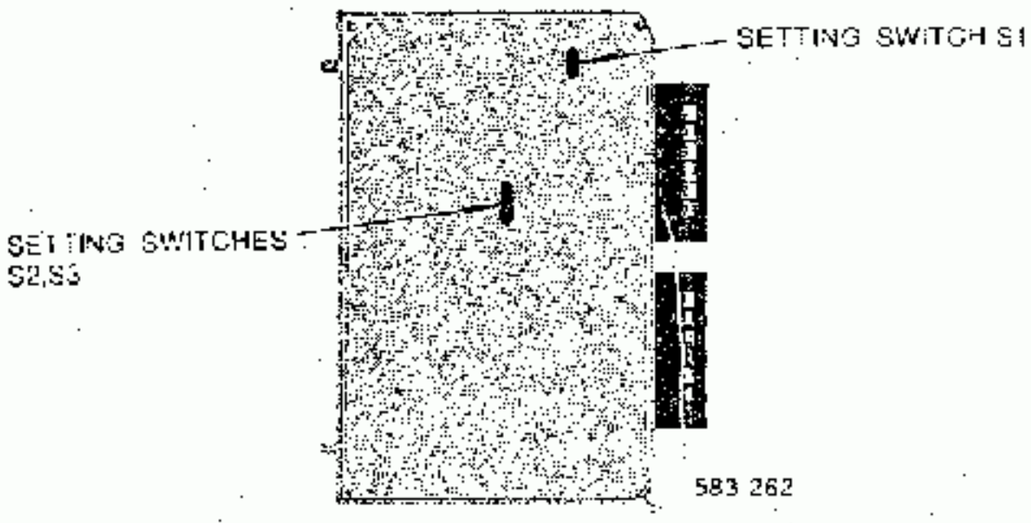


Fig. 3.8 Location of Setting Switches

3.6.1 Function of Setting Switch S1 (Response Frequency Selection)

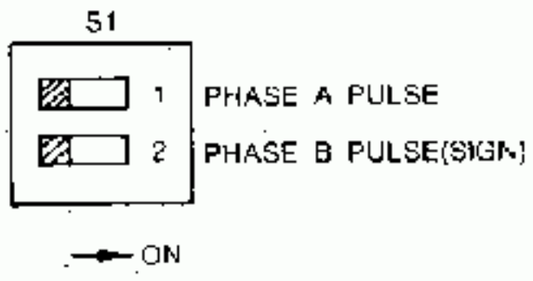
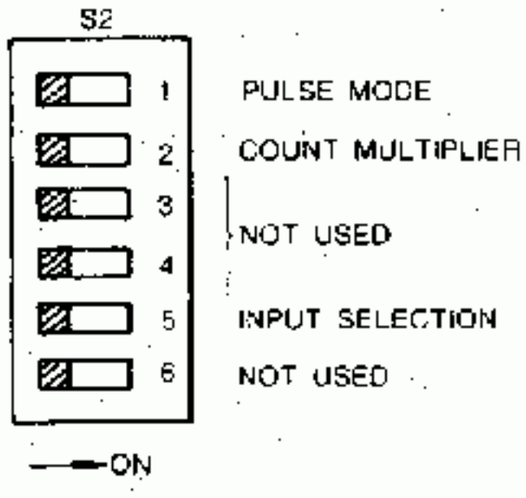


Table 3.12 Function of Setting Switch S1

Setting Switch	OFF	ON
S 1-1	40 kpps	400 pps
S 1-2	40 kpps	400 pps

Note: Be sure S1-1 and S1-2 are set equally.

3.6.2 Function of Setting Switch S2



(1) Input Pulse Selection

Table 3.13 Function of Setting Switch S2

Setting Switch	OFF	ON
S 2-1	Phases A and B	Pulse with sign
S 2-2	×1	×2
S 2-5	COUNT ENABLE	EXTERNAL RESET

(2) Setting of Hysteresis Width

Table 3.14 Setting of Hysteresis Width of S2

Setting Switch		Hysteresis Width
S 2-3	S 2-4	
OFF	OFF	0 pulse
ON	OFF	2 pulses
OFF	ON	5 pulses
ON	ON	10 pulses

(3) Notch Output Pattern Selection

Setting Switch	OFF	ON
S 2-6	Pattern A	Pattern B

Note: The hysteresis width and the notch output pattern are read-in by the module only when power is up.

3.6.3 Functions of Setting Switch S3 (Setting Mode Selection)

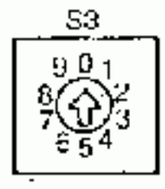


Table 3.15 Functions of Setting Switch S3

Setting Switch	Setting Mode
S 3-0	Decimal 6-digit, 1-notch, 2-register×1-scan (R84H)
S 3-1	Decimal 6 digit, 4-notch, 2-register×4-scan (R84H)
S 3-2	Decimal 6-digit, 4-notch, 8-register×1-scan (R84H)
S 3-3	Decimal 6-digit, 8-notch, 2-register×8-scan (R84H)
S 3-4	Decimal 6-digit, 8-notch, 8-register×2-scan (R84H)
S 3-5	Decimal 8-digit, 1-notch, 2-register×1-scan (U84, 584)
S 3-6	Decimal 8-digit, 4-notch, 2-register×4-scan (U84, 584)
S 3-7	Decimal 8-digit, 4-notch, 8-register×1-scan (U84, 584)
S 3-8	Decimal 8-digit, 8-notch, 2-register×8-scan (U84, 584)
S 3-9	Decimal 8-digit, 8-notch, 8-register×2-scan (U84, 584)

Note: Setting mode is read-in by the module only when power is up.

IMPORTANT

When the module is delivered, S1 and S2 for all the setting switches are OFF, and S3 is S3-0.

3.7 ELEMENT LAYOUT OF FRONT PANEL

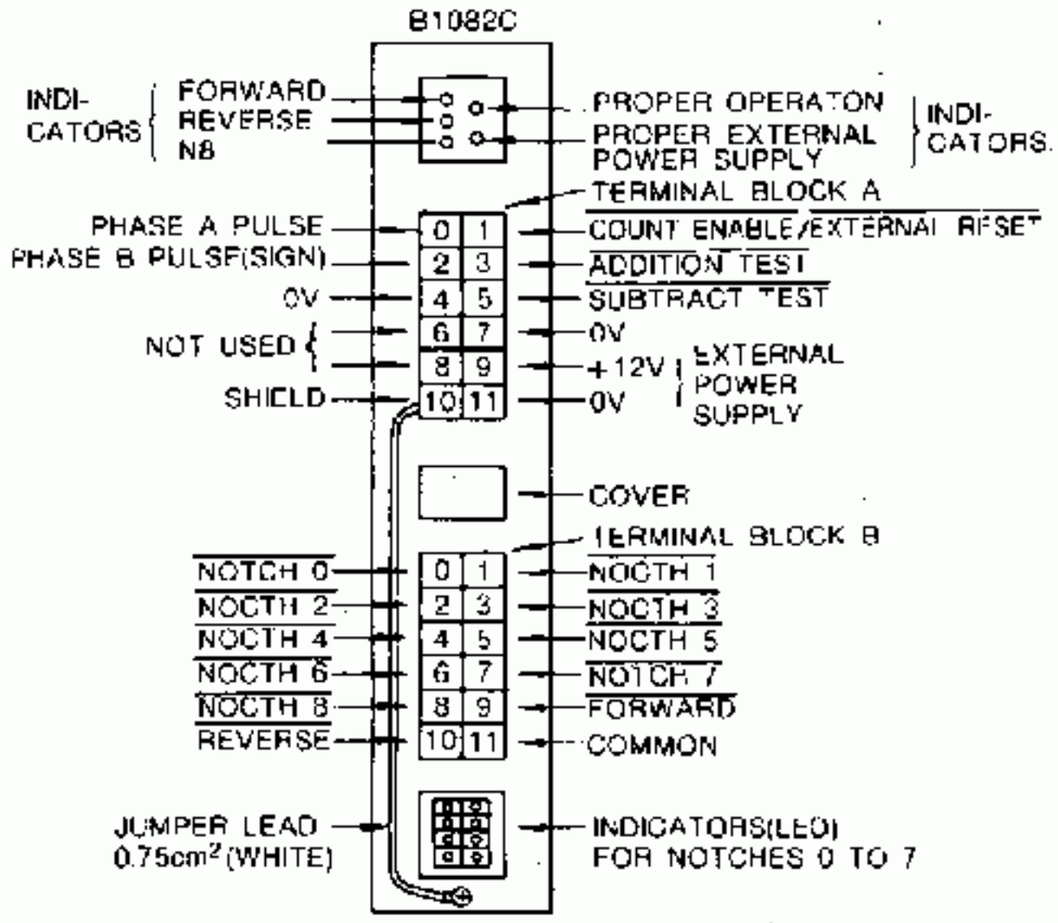


Fig. 3.9 Element Layout on Front Panel of B1082C

3.8 INPUT/OUTPUT ALLOCATION

3.8.1 R84H I/O Allocation

Similar to other I/O modules, B1082C requires I/O allocation to exchange signals with the R84H. For details of the I/O allocation, refer to Memocon-SC R84H DESIGNER'S REFERENCE MANUAL: SIE-C815-9.4. B1082C requires the following allocations.

- Discrete input relay: 16
- Input register: 2
- Discrete output coil: 16
- Output register: 2 or 8 (depending on setting mode)

The I/O allocation for B1082C is as follows:

I/O allocation table for input signals 41×× = [0 2 2]

Input register (binary)

Discrete input relay

I/O allocation table for output signals 40×× =

[0 2 2] ... For 2-register setting mode

[0 8 2] ... For 8-register setting mode

Output register (binary)

Discrete output coil

NOTE

Be sure to specify binary numbers to the input and output registers.

3.8.2 U84, U84J I/O Allocation

In the U84 or U84J I/O allocation, B1082C requires the same number of I/O points as those of the R84H and the 584.

- Discrete input relay : 16
- Input register : 2
- Discrete output coil : 16
- Output register : 2 or 8 (depending on setting mode)

Reference number must be specified as well.

Fig. 3.10 shows a sample U84, U84J I/O allocation on CRT screen of P190 programming panel, where B1082C is inserted into slot 1 of rack 2 in U84, U84J channel 1.

CHANNEL : 01 RACK : 2

INPUT

SLOT	DISCRETE REF #	DISCRETE POINTS	REGISTER REF #	REGISTER BCD	REGISTER BINARY
1	.....	INHIBIT	.....	INHIBIT	INHIBIT
2	10057	16	30020	INHIBIT	2
3	.....	INHIBIT	.....	INHIBIT	INHIBIT

CHANNEL : 01 RACK : 2

OUTPUT

SLOT	DISCRETE REF #	DISCRETE POINTS	REGISTER REF #	REGISTER BCD	REGISTER BINARY
1	.....	INHIBIT	.....	INHIBIT	INHIBIT
2	00057	16	40019	INHIBIT	8
3	.....	INHIBIT	.....	INHIBIT	INHIBIT

Fig. 3.10 Sample U84, U84J I/O Allocation

3.8.3 584 I/O Allocation

Where 1000 series I/O module is connected to Memocon-SC584, an I/O adapter, Type DISCT-J1040 is required. I/O allocation must be set for both the 584 and the adapter. For the adapter I/O allocation, refer to "Memocon-SC584 1000 SERIES I/O ADAPTER"(SIE-C815-7.80).

B1082C requires the following number of I/O points.

- Discrete input relay : 16
- Input register : 2
- Discrete output coil : 16
- Output register : 2

A sample 584 I/O allocation is shown in Fig. 3.11, using CRT screen of P190 programming panel. Fig. 3.12 lists an examples of I/O allocation conversion table for the J1040 adapter, where B1082C is inserted into slot 01 of J1040.

CHANNEL : 01

	INPUT			OUTPUT	
SLOT	REF #	TYPE	SLOT	REF #	TYPE
1	10001	DISCRETE	1	00001	DISCRETE
2	30001	BIN REG	2	40001	BIN REG
3	30002	BIN REG	3	40002	BIN REG
4	.....	INHIBIT	4	40003	BIN REG
5	.....	INHIBIT	5	40004	BIN REG
6	.....	INHIBIT	6	40005	BIN REG
7	.....	INHIBIT	7	40006	BIN REG
8	.....	INHIBIT	8	40007	BIN REG

CHANNEL : 02

	INPUT			OUTPUT	
SLOT	REF #	TYPE	SLOT	REF #	TYPE
1	.....	INHIBIT	1	40008	BIN REG
2	.....	INHIBIT	2	.....	INHIBIT
3	.....	INHIBIT	3	.....	INHIBIT

Note: Be sure to specify binary numbers to the input and output registers.

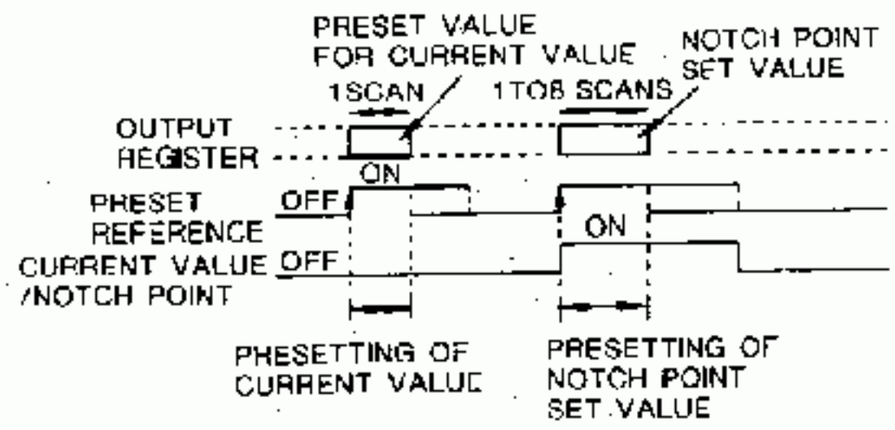
Fig. 3.11 Sample 584 I/O Allocation

		Input				Output			
		584		1000 Series I/O		584		1000 Series I/O	
	SLOT	Input		R/D	SLOT	SLOT	Output	R/D	SLOT
Odd Channel	1	10001		D	01	1	00001	D	01
	2	30001		R	01	2	40001	R	01
	3	30002		R	01	3	40002	R	01
	4	INHIBIT		—	—	4	40003	R	01
	5	INHIBIT		—	—	5	40004	R	01
	6	INHIBIT		—	—	6	40005	R	01
	7	INHIBIT		—	—	7	40006	R	01
	8	INHIBIT		—	—		40007	R	01
Even	1	INHIBIT		—		Even	40008	R	01
	2	INHIBIT		—		2	INHIBIT	—	—
	3	INHIBIT		—		3	INHIBIT	—	

Fig. 3.12 Example of I/O Allocation Conversion Table for J1040 Adapter

3.9 PRESETTING

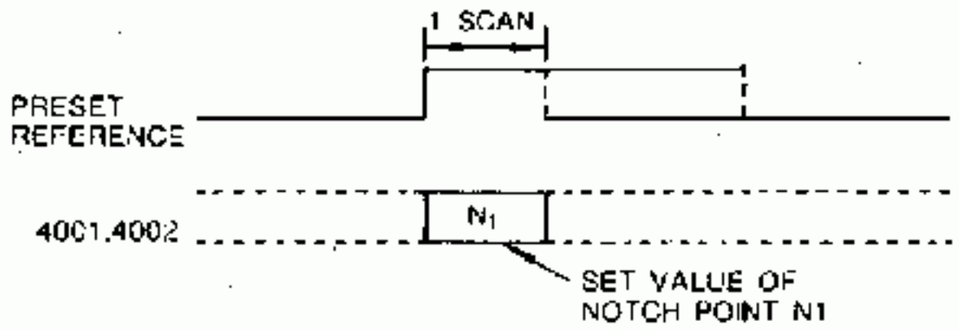
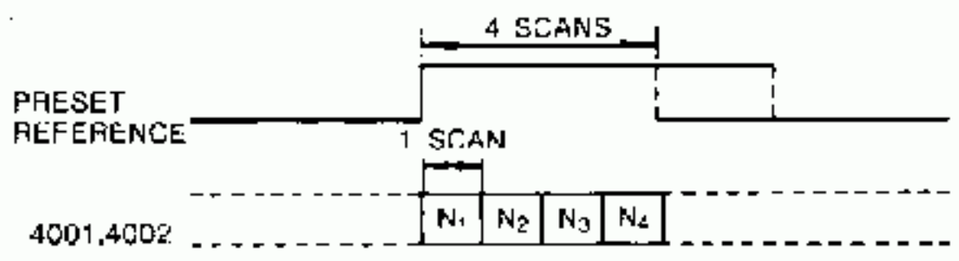
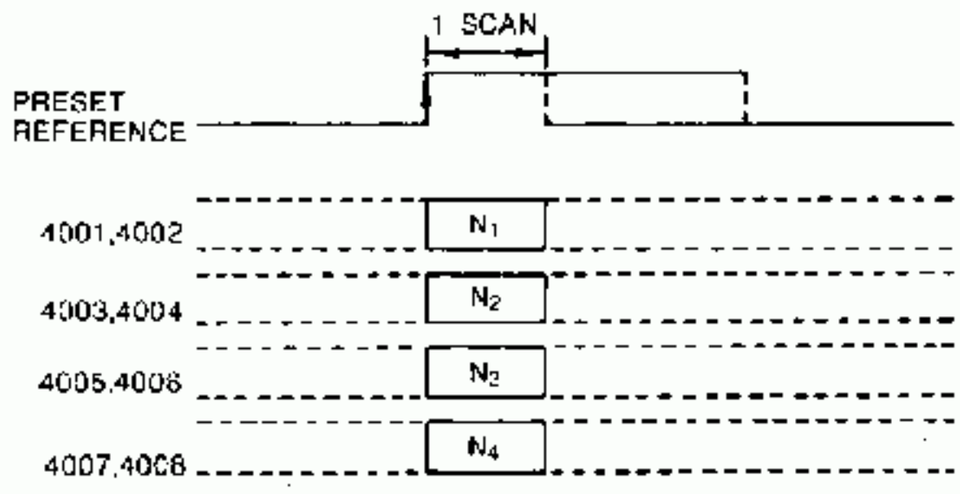
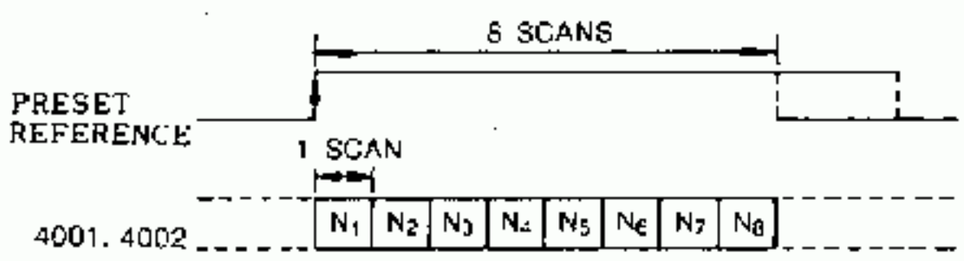
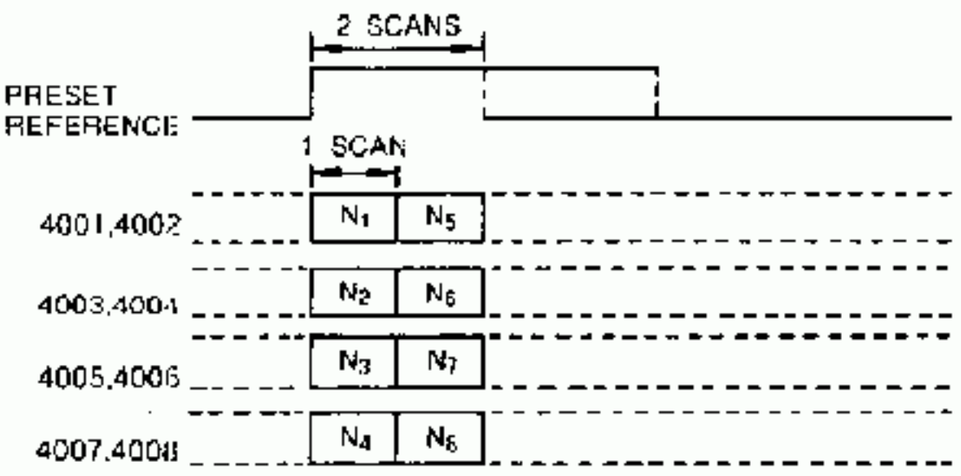
B1082C is preset for either the current value and/or the notch point set value. See Fig. 3.13



Note:
1. With the current value presetting, the same applies as for B1081C
2. To preset the notch point set value, keep PRESET REFERENCE and CURRENT VALUE/NOTCH POINT turned ON for a number of scans more than specified by the setting mode. If less than the specified number of scans, it will constitute a format error, and presetting is impossible. (The notch point set value remains uchanged from the existing value). Also the ERROR input relay is turned on. To reset the ERROR, execute MODULE RESET, and then, preset properly.
3. When presetting notch point set values, the output register contents must be controlled according to Table 3.16, because the preset sequence is specified by the setting mode.

Fig. 3.13 B1082C Presetting Operation

Table 3.16 Preset Sequence by Setting Mode (R84H)

Setting Mode		Preset Sequence of Notch Point Set Value
0	1-Notch Setting 2-Register × 1-Scan	
1	4-Notch Setting 2-Register × 4-Scan	
2	4-Notch Setting 8-Register × 1-Scan	
3	8-Notch Setting 2-Register × 8-Scan	
4	8-Notch Setting 8-Register × 2-Scan	

Note:

1. The use of 4001 to 4008 output registers is assumed. Note that 4001 and 4002 can also be used for current value presetting.
2. Determine the setting mode on the basis of the system requirements, such as to reduce the required number of notches and output registers, or to reduce the number of setting scans.
3. While CURRENT VALUE/NOTCH POINT is OFF, the current value of counter is monitored, as with B1081C.
4. While CURRENT VALUE/NOTCH POINT is ON, the notch point set value is monitored, and the set value at the notch point specified by the three output coils with MONITOR 0, MONITOR 1 and MONITOR 2 is monitored by the input register. However, while the notch point set value is under presetting in the module, the content of the input register cannot be determined.

3.10 LADDER DIAGRAM EXAMPLES

3.10.1 R84H Ladder Diagram Examples

(1) 1-Notch Setting, 2-Register × 1-Scan
(4-Notch Setting, 8-Register × 8-Scan)

- Discrete output: 0001 - 0016
- Output register: 4001, 4002
- 4101: Preset value for current value (high order)
- 4102: Preset value for current valuc (low order)
- 4151: Notch point N1 set value (high order)
- 4152: Notch point N1 set value (low order)

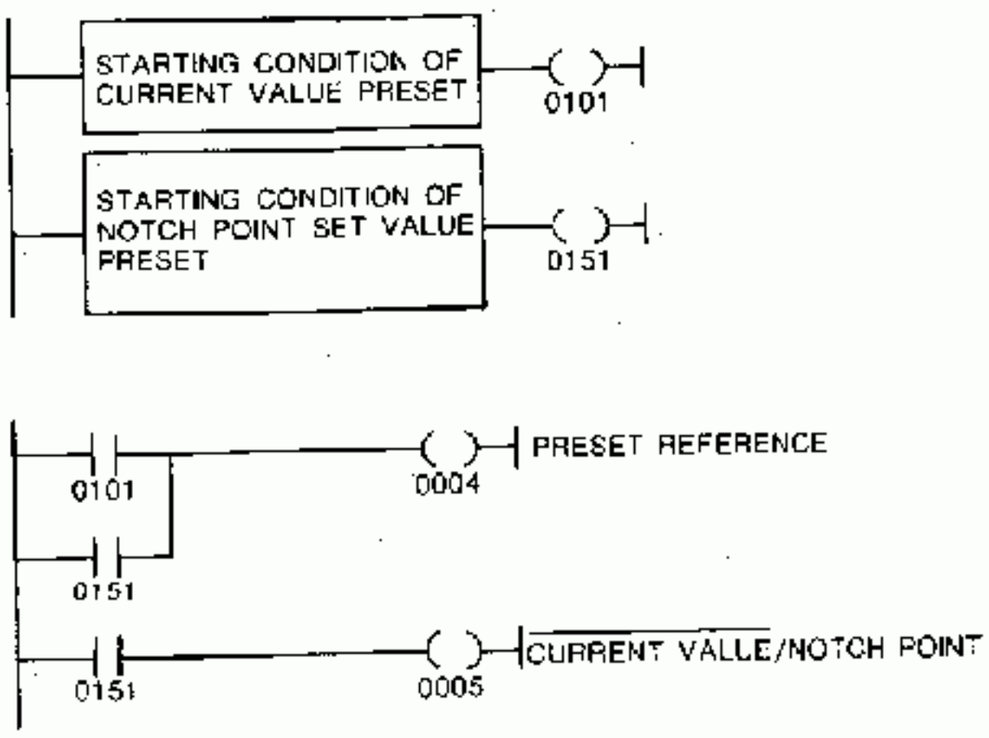


Fig. 3.14 Example 1 of R84H Ladder Diagram

For 4- notch setting, 8-register × 1 scan, add the following.

- Output register: 4003 - 4008
- 4153: Notch point N2 set value (high order)
- 4154: Notch point N2 set value (low order)
- 4155: Notch point N3 set value (high order)
- 4156: Notch point N3 set value (low order)
- 4157: Notch point N4 set value (high order)
- 4158: Notch point N4 set value (low order)

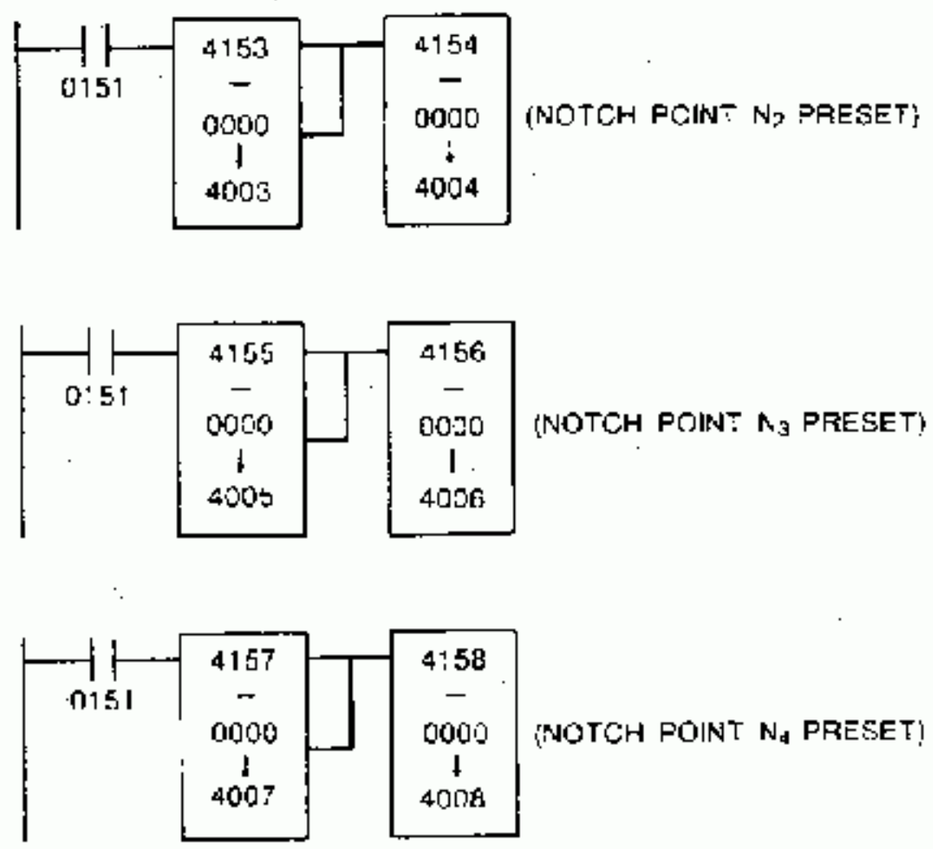


Fig. 3.15 Example 2 of R84H Ladder Diagram

(2) 4-Notch Setting, 2-Register × 4-Scan
(8-Notch Setting, 2-Register × 8-Scan)

- Discrete output: 0001 - 0016
- Output register: 4001, 4002
- 4101: Preset value for current value (high order)
- 4102: Preset value for current value (low order)
- 4151: Notch point N1 set value (high order)
- 4152: Notch point N1 set value (low order)
- 4153: Notch point N2 set value (high order)
- 4154: Notch point N2 set value (low order)
- 4155: Notch point N3 set value (high order)
- 4156: Notch point N3 set value (low order)
- 4157: Notch point N4 set value (high order)
- 4158: Notch point N4 set value (low order)

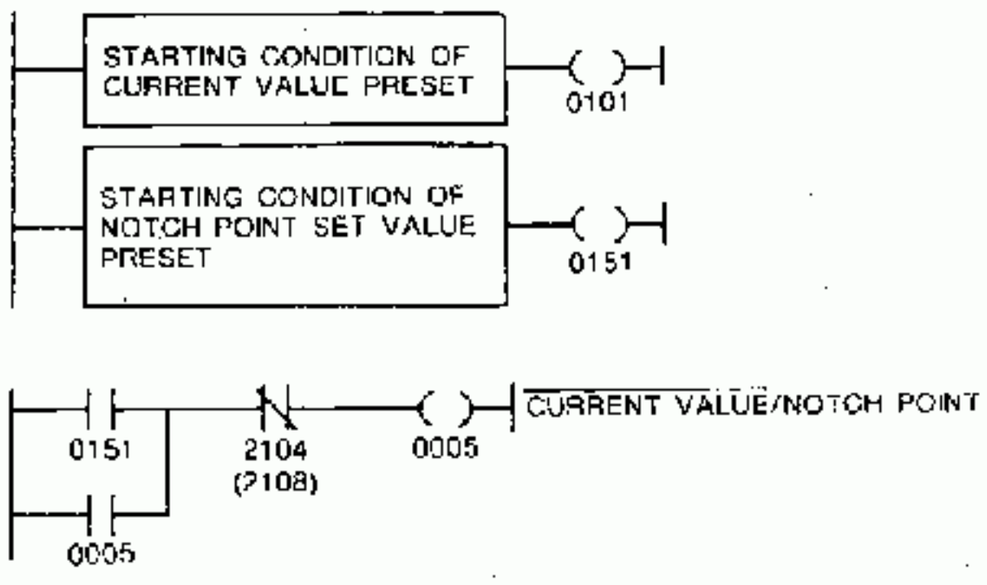


Fig. 3.16 Example 3 of R84H Ladder Diagram

For 8-notch setting, 2-register × 8-scan, add the following.

- 4159: Notch point N5 set value (high order)
- 4160: Notch point N5 set value (low order)
- 4161: Notch point N6 set value (high order)
- 4162: Notch point N6 set value (low order)
- 4163: Notch point N7 set value (high order)
- 4164: Notch point N7 set value (low order)
- 4165: Notch point N8 set value (high order)
- 4166: Notch point N8 set value (low order)

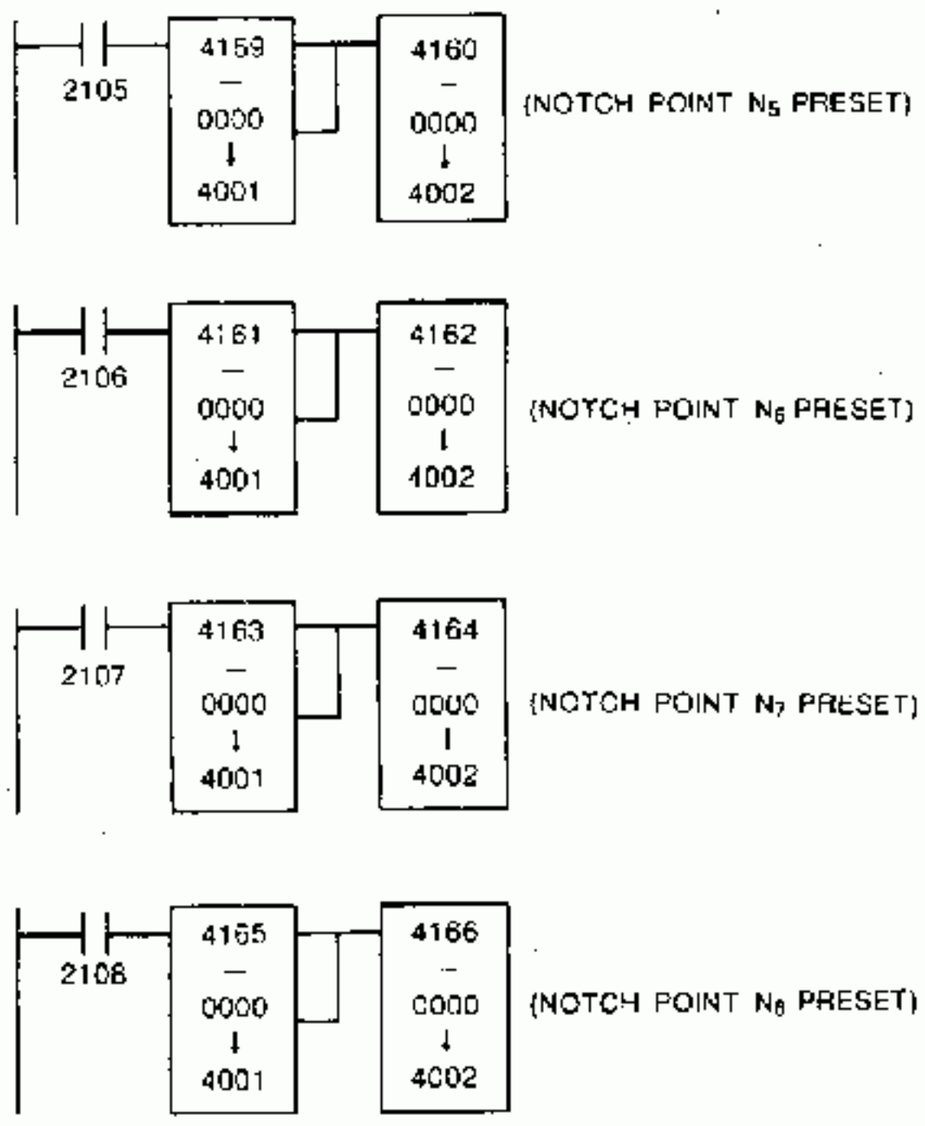
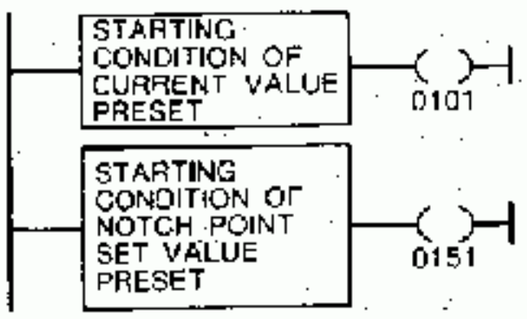
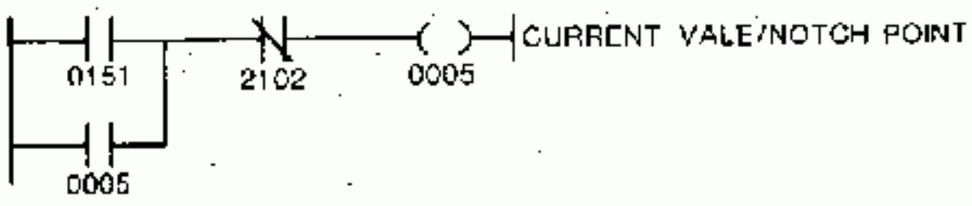


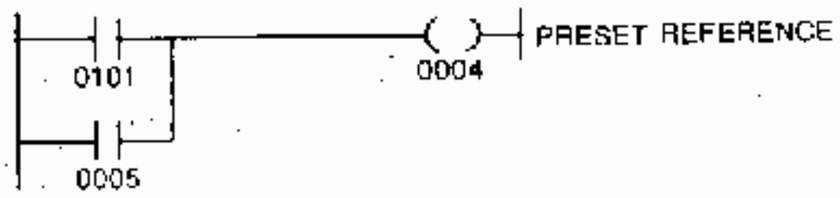
Fig. 3.17 Example 4 of R84H Ladder Diagram

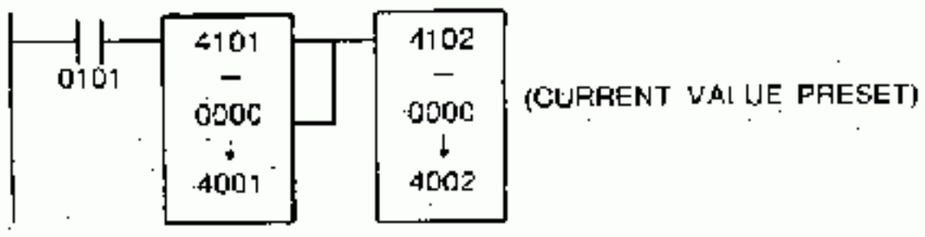
(3) 8-Notch Setting, 8-Register × 2-Scan

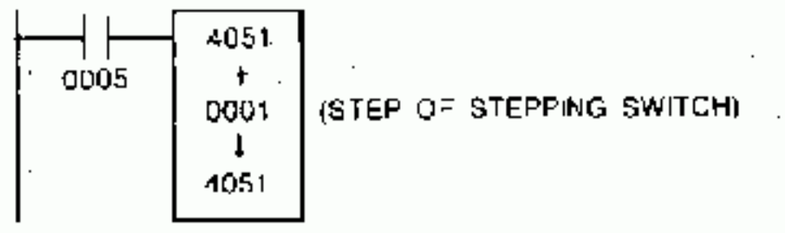
- Discrete output: 0001 - 0016
- Output register: 4001 - 4008
- 4101: Preset value for current value (high order)
- 4102: Preset value for current value (low order)
- 4151: Notch point N1 set value (high order)
- 4152: Notch point N1 set value (low order)
- 4153: Notch point N2 set value (high order)
- 4154: Notch point N2 set value (low order)
- 4155: Notch point N3 set value (high order)
- 4156: Notch point N3 set value (low order)
- 4157: Notch point N4 set value (high order)
- 4158: Notch point N4 set value (low order)
- 4159: Notch point N5 set value (high order)
- 4160: Notch point N5 set value (low order)
- 4161: Notch point N6 set value (high order)
- 4162: Notch point N6 set value (low order)
- 4163: Notch point N7 set value (high order)
- 4164: Notch point N7 set value (low order)
- 4165: Notch point N8 set value (high order)
- 4166: Notch point N8 set value (low order)











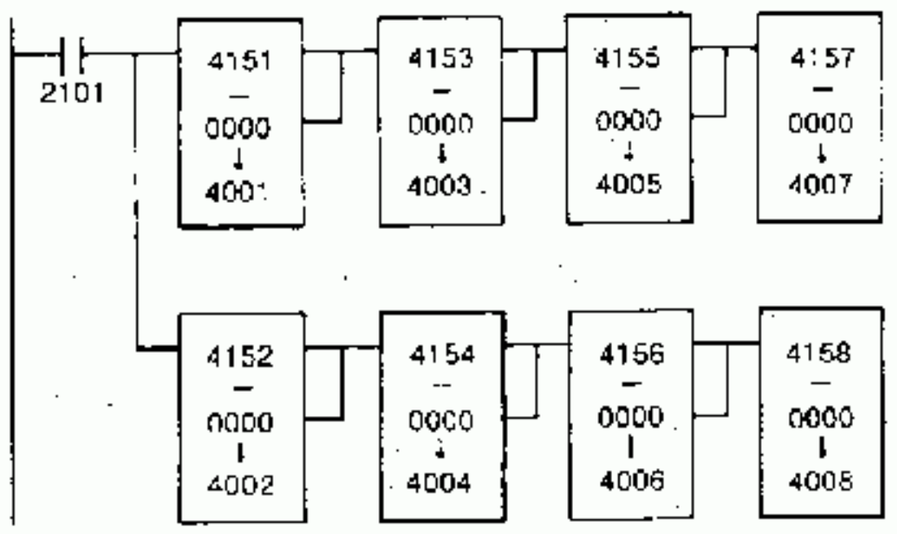
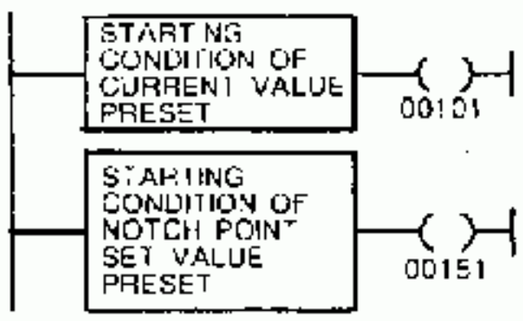


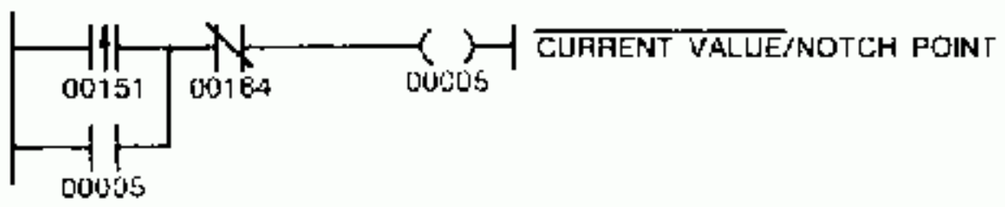
Fig. 3.18 Example 5 of R84H Ladder Diagram

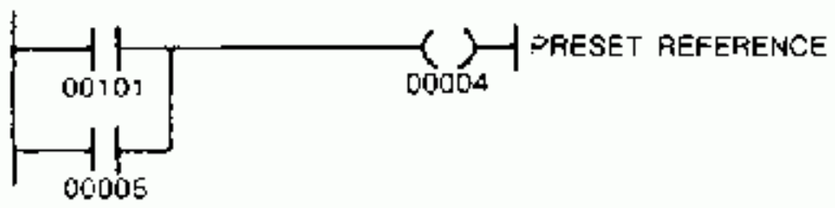
3.10.2 U84, U84J, 584 Ladder Diagram Examples

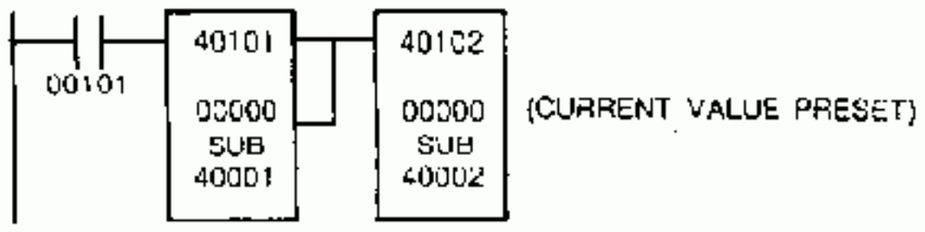
(1) 4-Notch Setting, 2-Register × 4-Scan

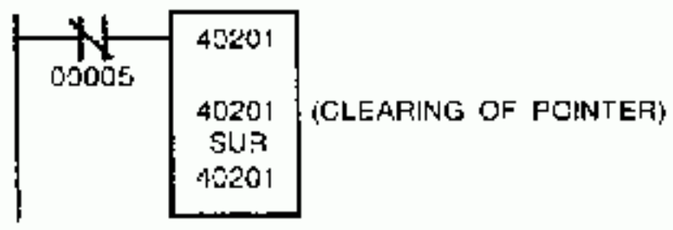
- Discrete output : 00001 - 00016
- Output register : 40001, 40002
- 40101 : Preset value for current value (high order)
- 40102 : Preset value for current value (low order)
- 40151 : Notch point N1 set value (high order)
- 40152 : Notch point N1 set value (low order)
- 40153 : Notch point N2 set value (high order)
- 40154 : Notch point N2 set value (low order)
- 40155 : Notch point N3 set value (high order)
- 40156 : Notch point N3 set value (low order)
- 40157 : Notch point N4 set value (high order)
- 40158 : Notch point N4 set value (low order)
- 40201 : Pointer
- 40100 : Working register

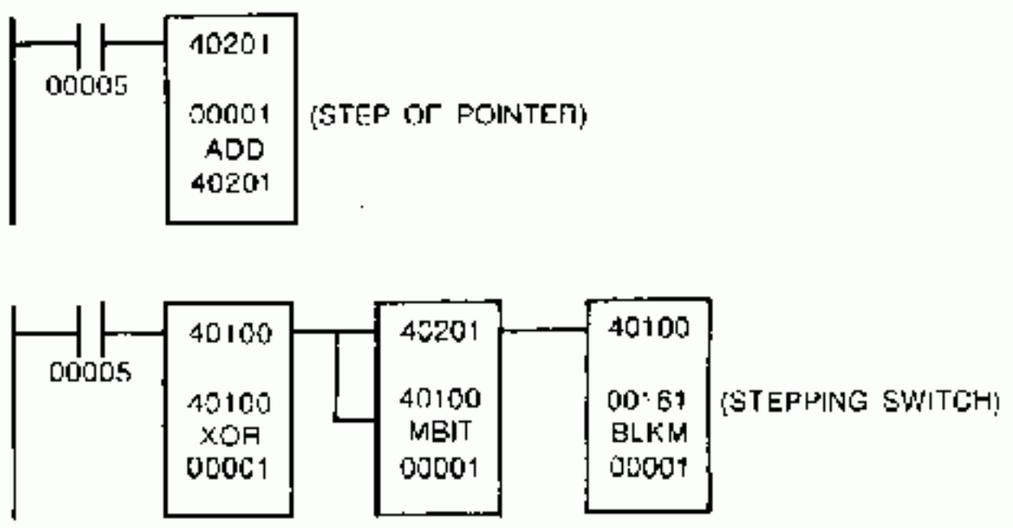












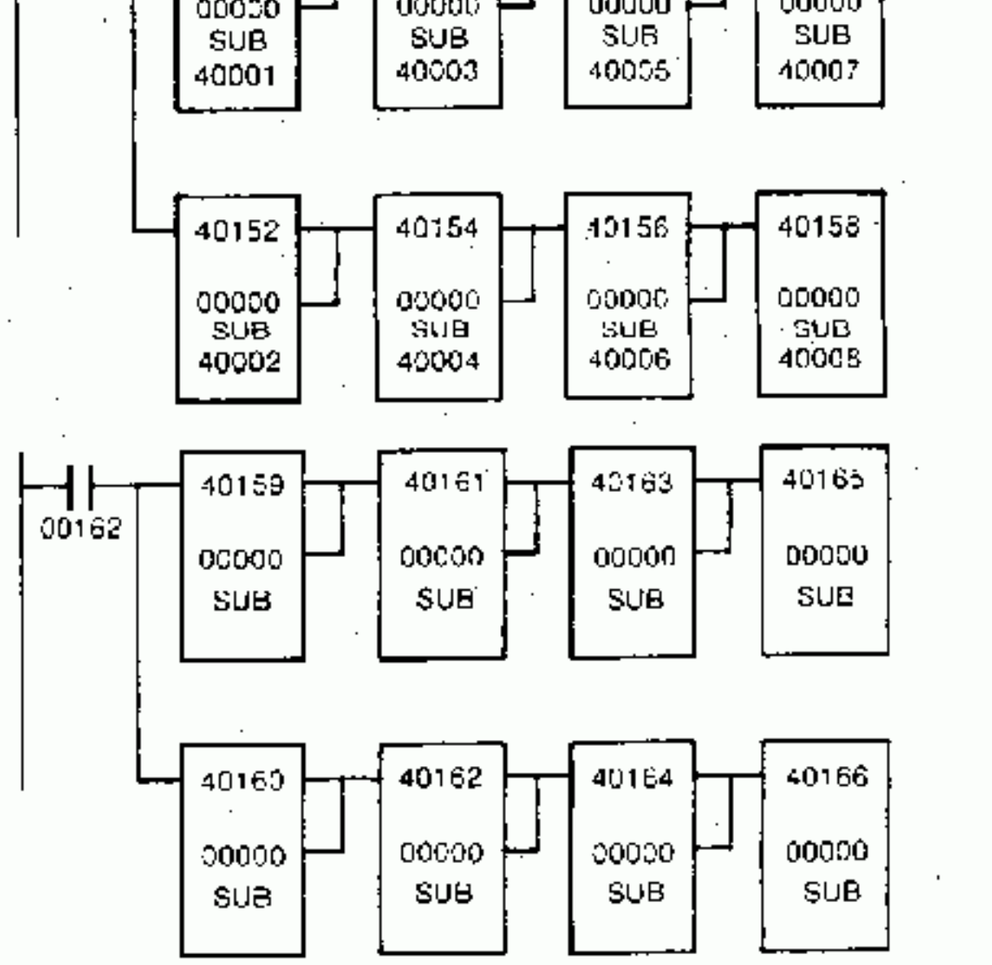
Note: Coils 00165 to 00176 cannot be used for other applications.

Fig. 3. 19 Example 1 of U84/U84J/584 Ladder Diagram

3.10.2 U84, 584 Ladder Diagram Examples (Cont'd)

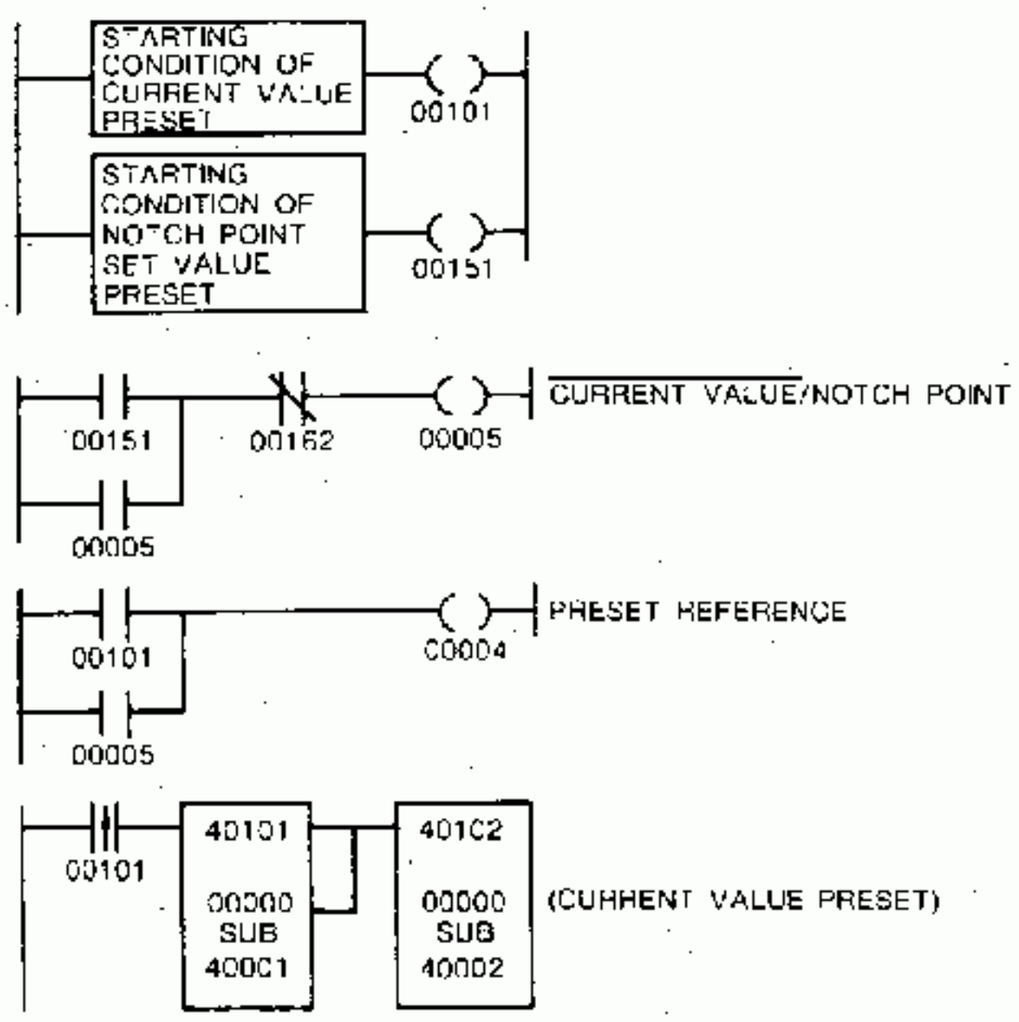
(2) 8-Notch Setting, 8-Register × 2-Scan

- Discrete output : 00001 - 00016
- Output register : 40001 - 40008
- 40101 : Preset value for current value (high order)
- 40102 : Preset value for current value (low order)
- 40151 : Notch point N1 set value (high order)
- 40152 : Notch point N1 set value (low order)
- 40153 : Notch point N2 set value (high order)
- 40154 : Notch point N2 set value (low order)
- 40155 : Notch point N3 set value (high order)
- 40156 : Notch point N3 set value (low order)
- 40157 : Notch point N4 set value (high order)
- 40158 : Notch point N4 set value (low order)
- 40159 : Notch point N5 set value (high order)
- 40160 : Notch point N5 set value (low order)
- 40161 : Notch point N6 set value (high order)
- 40162 : Notch point N6 set value (low order)
- 40163 : Notch point N7 set value (high order)
- 40164 : Notch point N7 set value (low order)
- 40165 : Notch point N8 set value (high order)
- 40166 : Notch point N8 set value (low order)
- 40201 : Pointer
- 40100 : Working register



Note: Coils 00163 to 00176 cannot be used for other applications.

Fig. 3.20 Example 2 of U84/584 Ladder Diagram



3.11 CARRY AND BORROW

When more than 6 digits places are required for counting, digits can be carried and borrowed from the module. Figs. 3.21 and 3.22 show examples of ladder diagrams.

Discrete input: 1001 - 1016

Register input: 3001, 3002

4081: High-order digit register

4100: Working register

4081	3001	3002	9-digit decimal
High-order 3 digits	Middle-order 3 digits	Low-order 3 digits	0 - 999999999

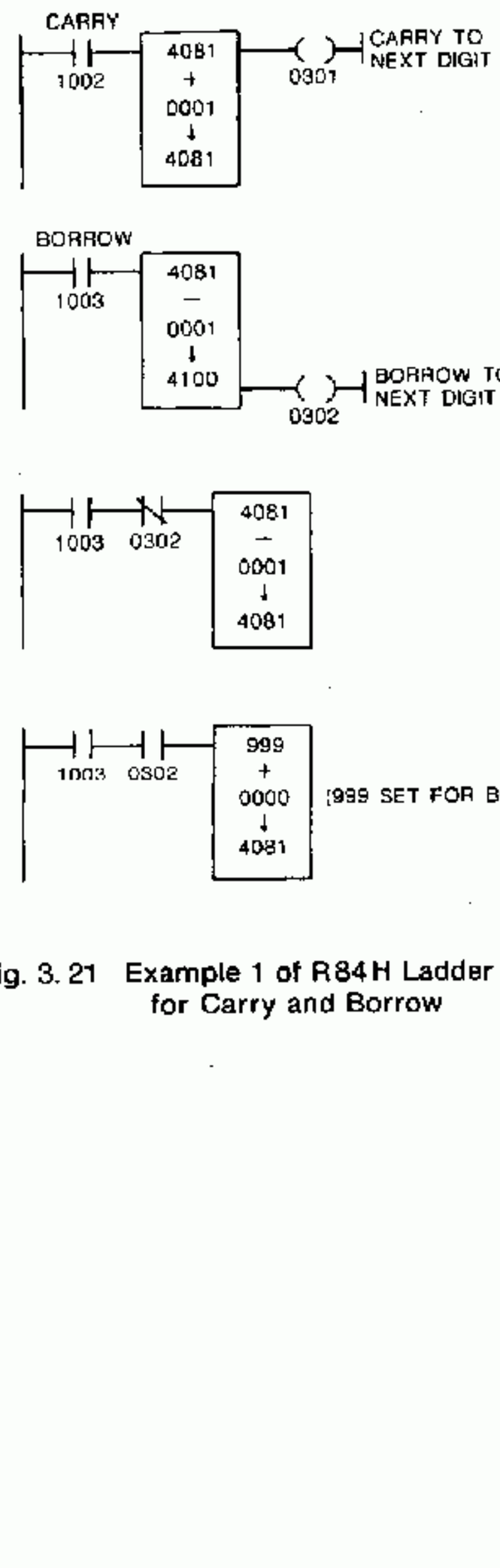
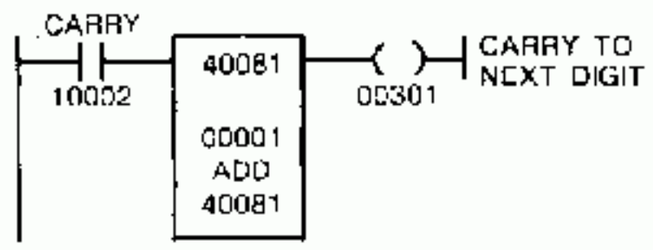


Fig. 3.21 Example 1 of R84H Ladder Diagram for Carry and Borrow

Discrete input: 10001-10016
Register input: 30001,30002
High-order digit register: 40081
Working register: 40100



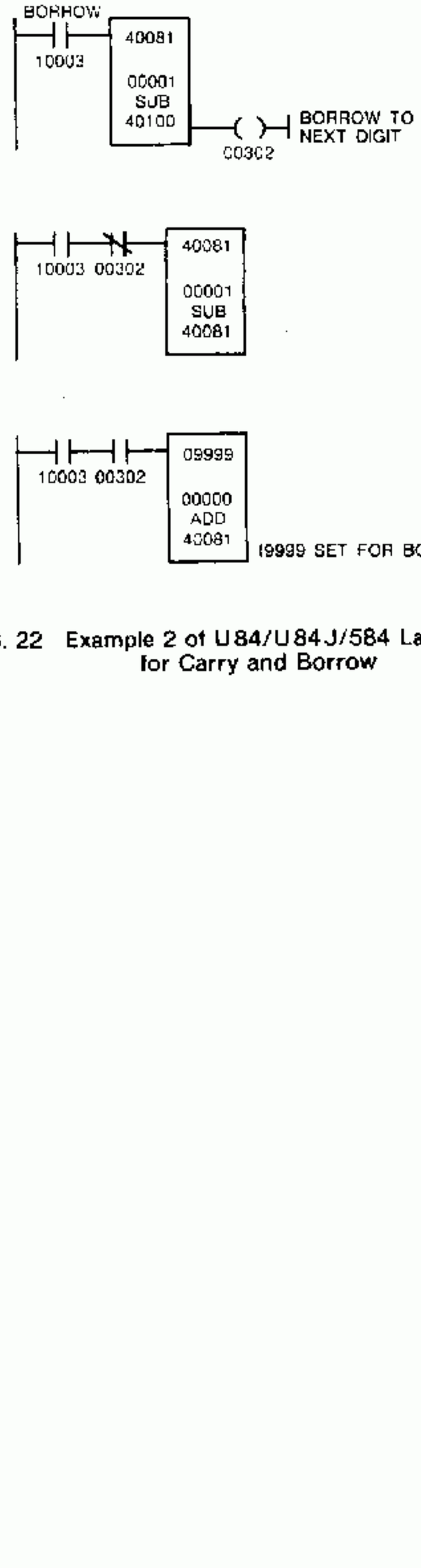


Fig. 3.22 Example 2 of U84/U84J/584 Ladder Diagram for Carry and Borrow

3.12 NOTCH OUTPUT

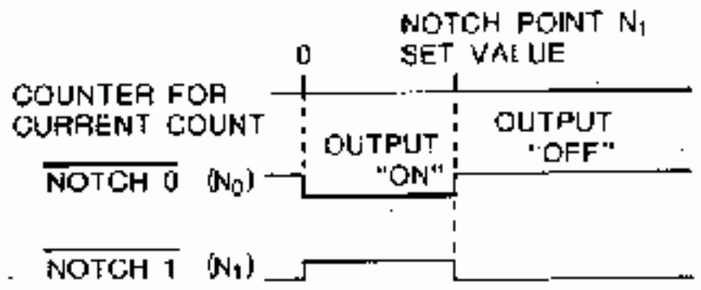
3.12.1 Patterns A and B

Preset counter module BI082C is provided with two types of notch outputs: pattern A and pattern B. The notch output for pattern A or B is selected by the setting switch S2 on the side of the module. For pattern A, the notch output form is the same regardless of forward/reverse running, but for pattern B, it is different depending on forward/reverse running.

3.12.2 Pattern A

(1) Basic Form of Notch Output

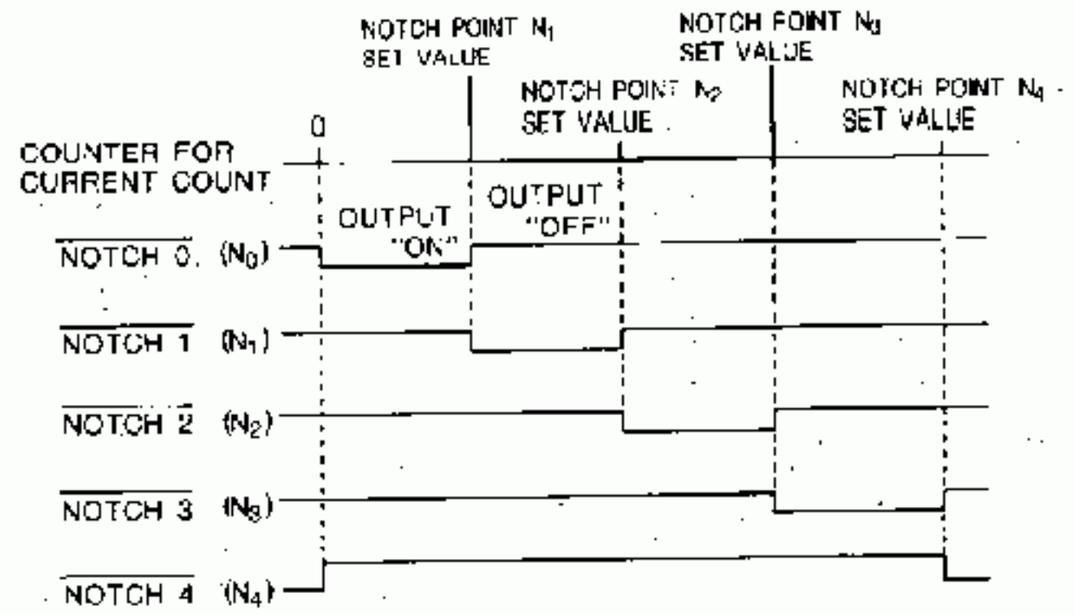
• 1-notch setting



Note: NOTCH 2 (N2) to NOTCH 8 (N8) are always OFF.

Fig. 3.23 1-Notch Output Setting

• 4-notch setting



Note: NOTCH 5 (N5) to NOTCH 8 (N8) are always OFF.

Fig. 3.24 4-Notch Output Setting

• 8-notch setting

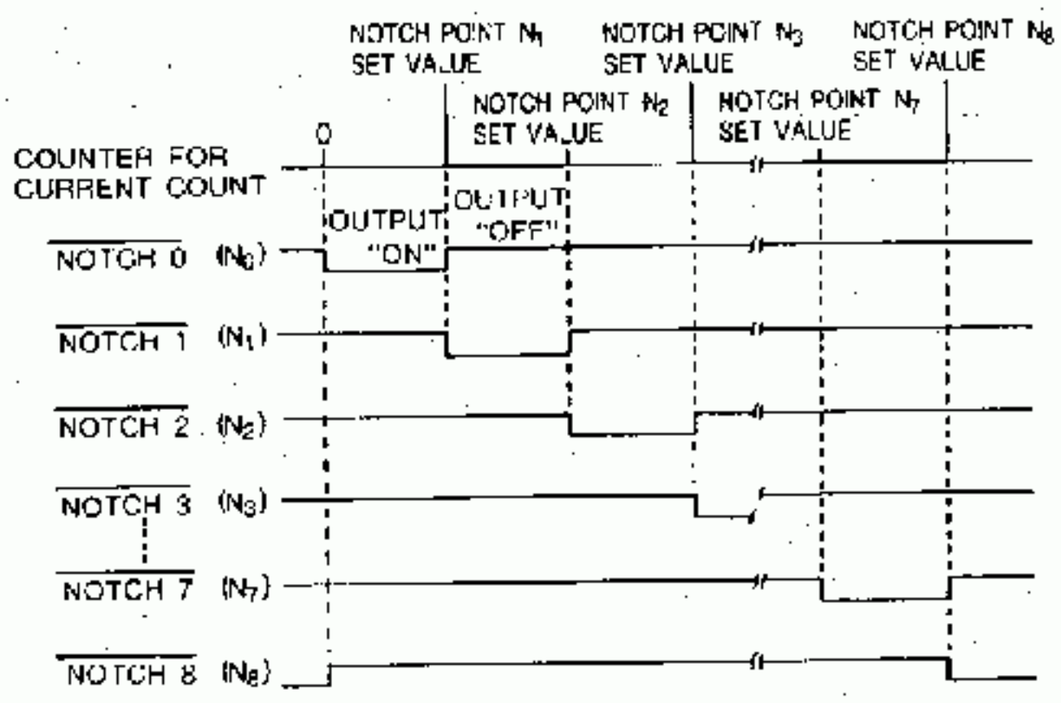


Fig. 3.25 8-Notch Output Setting

Note the following, as to the 1-notch, 4-notch and 8-notch settings.

- After turning on the power, or after executing module resetting, no notch output is possible until a notch point set value is preset.
- The switching of each notch output is not influenced by the counting direction of current value counter (adding or subtracting).

(2) Modification of Notch Output

The case of a 4-notch setting is described below. The same concept applies in the case of an 8-notch setting.

• possible same set values

Example: Notch point N2 = Notch point N3

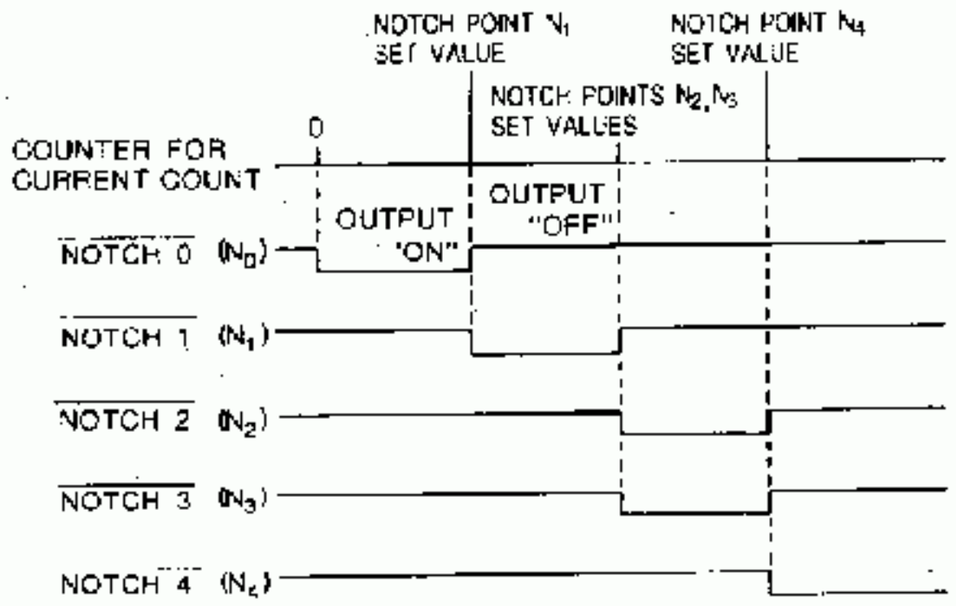


Fig. 3.26 Same Set Value (N2=N3)

• free set-value sizes

Example: Notch point N4 < Notch point N1 < Notch point N3 < Notch point N2

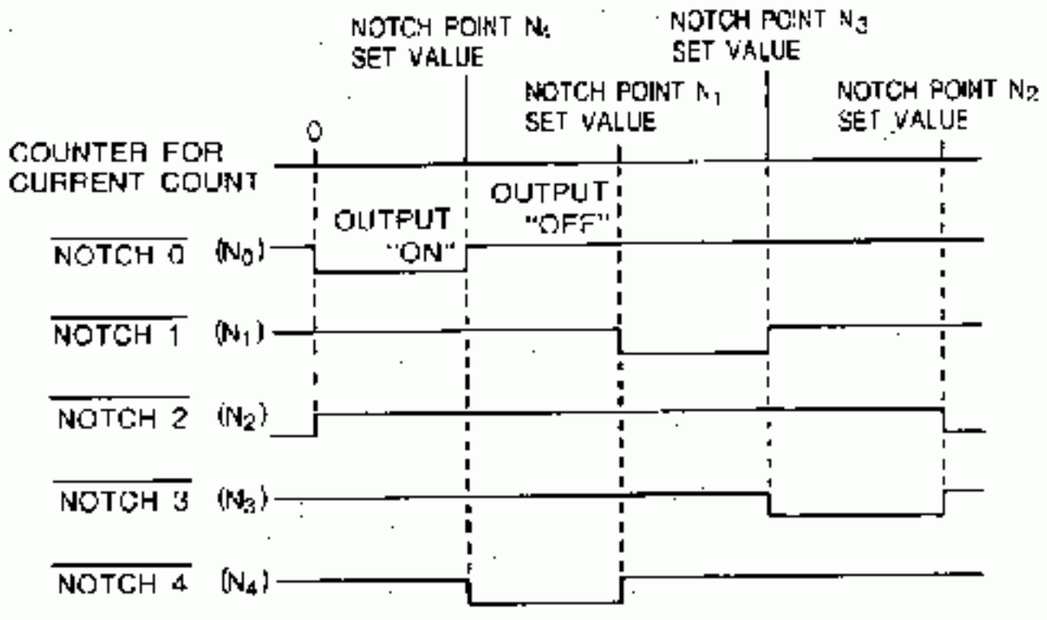


Fig. 3.27 Free Set-value Sizes Regardless of Notch Point N Sequence

NOTE

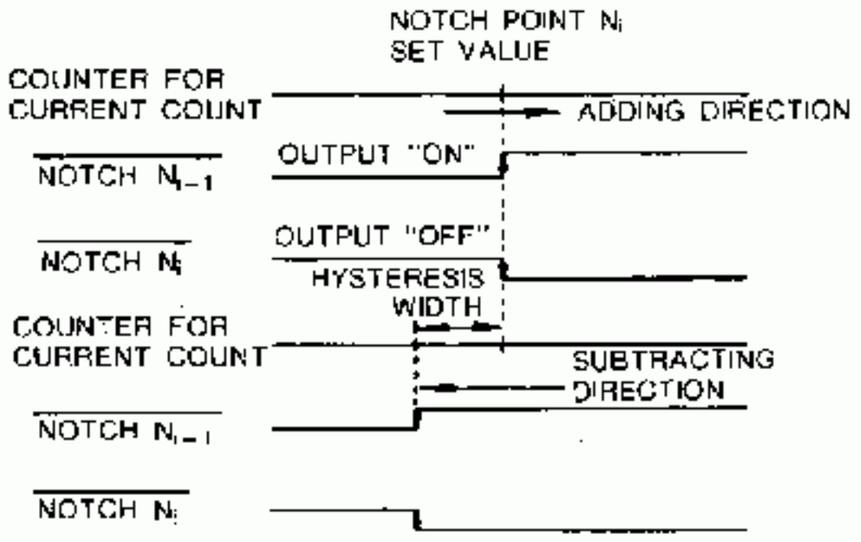
1. Notch output when not in use should be set to 0. In this case, the notch output results in no operation.

2. No notch output is ON until presetting notch point is done after turning power on or resetting a module.

3. In Pattern A, $\overline{\text{NOTCH 0}}$ (NO) is always output while current value of the counter ranges from 0 to the least notch point set value. Switching of each notch output is executed regardless of counting direction (addition/subtraction) of the current value counter.

(3) Hysteresis Width

When the setting switch S2 is used to set the hysteresis width, a hysteresis width is given to the notch output switching process.



Note:
1. The hysteresis width is effective commonly to all the notch output switchings.
2. When 0 pulse is set for the hysteresis width, the width becomes zero.

Fig. 3.28 Hysteresis Width

(4) Notch Output near Carry or Borrow

The notch output near CARRY and BORROW becomes endless.

Note: Hysteresis is in effective to the notch output switching near CARRY and BORROW, even if the hysteresis width is set.

Fig. 3.29 Notch Output near Carry or Borrow

3.12.3 Pattern B

(1) Basic Form of Notch Output

• 1-notch setting

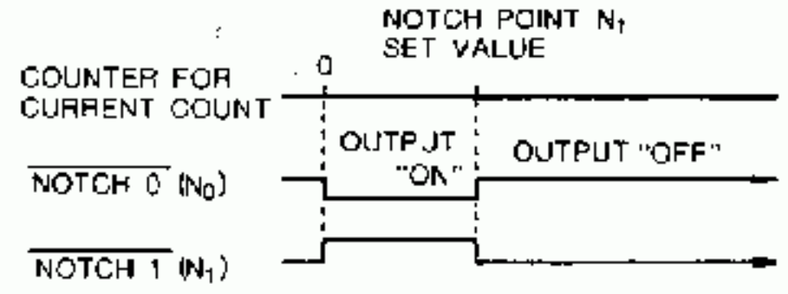
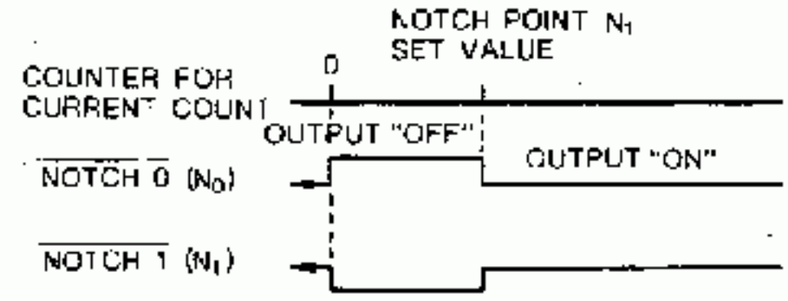


Fig. 3.30 When Output Coil ON for Forward Running



Note: $\overline{\text{NOTCH 2}}$ (N2) to $\overline{\text{NOTCH 8}}$ (N8) are always OFF.

Fig. 3.31 When Output Coil ON for Reverse Running

• 4-notch setting

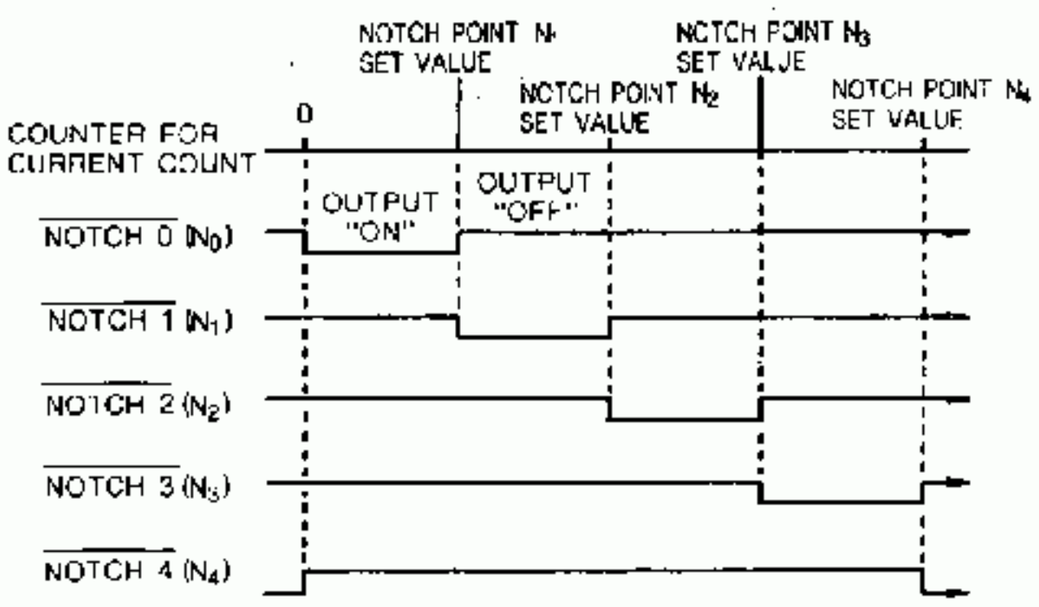
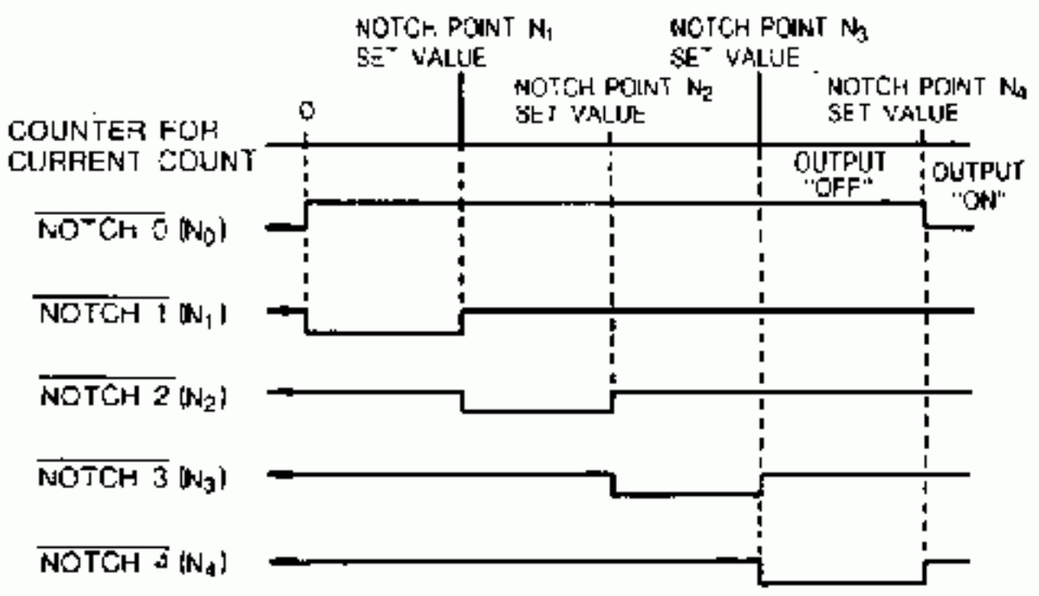


Fig. 3.32 When Output Coil ON for Forward Running



Note: $\overline{\text{NOTCH 5}}$ (N5) to $\overline{\text{NOTCH 8}}$ (N8) are always OFF.

Fig. 3.33 When Output Coil ON for Reverse Running

3. 12. 3 Pattern B (Cont'd)

- 8-notch setting

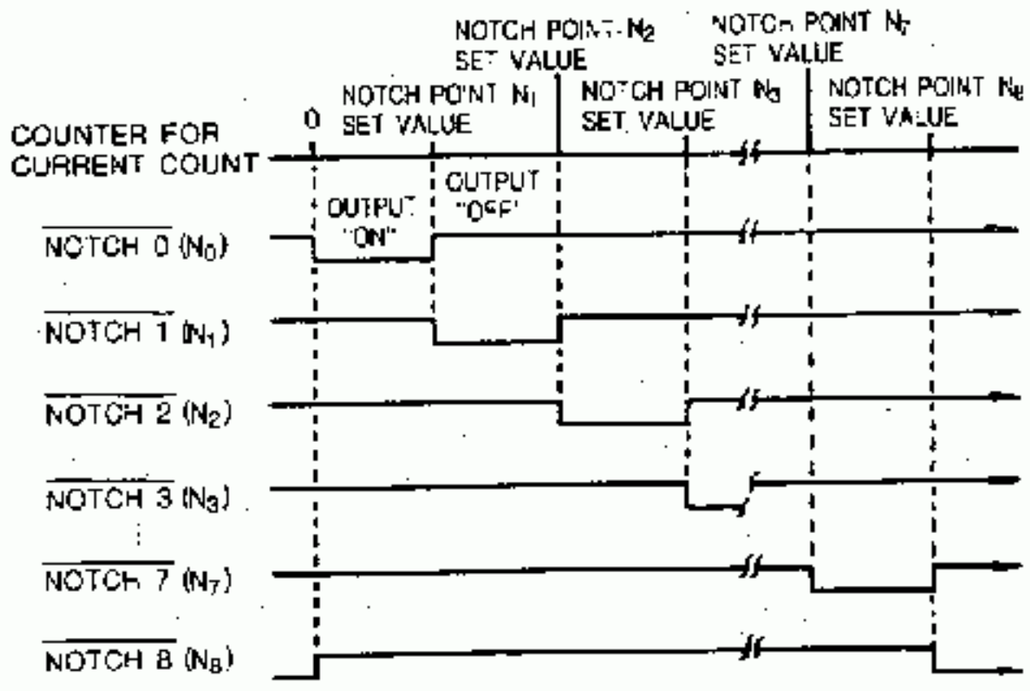


Fig. 3.34 When Output Coil ON for Forward Running

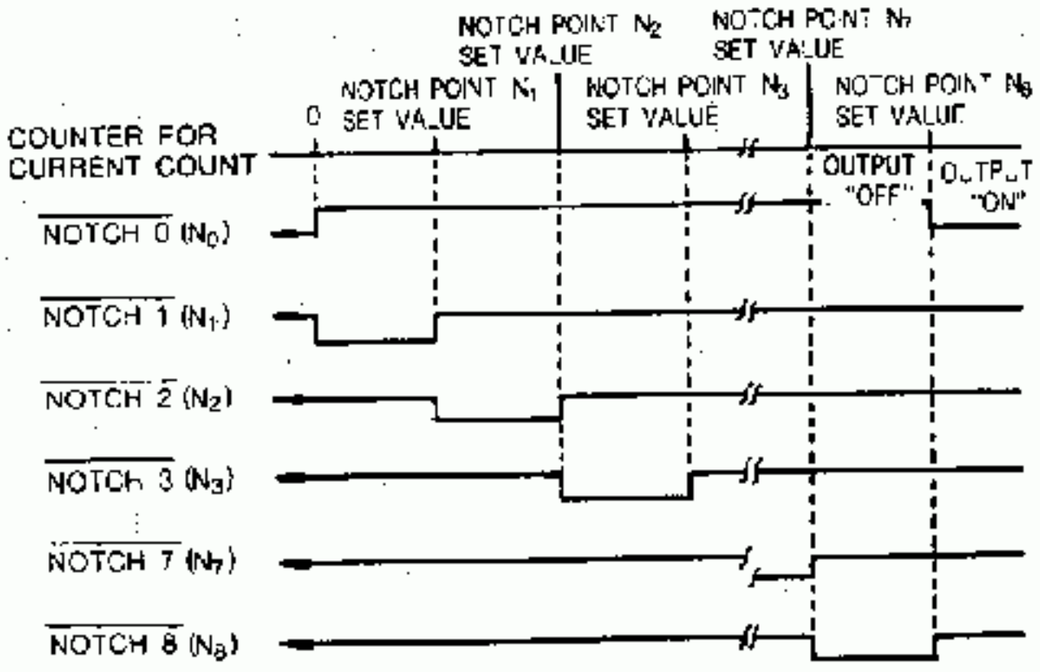


Fig. 3.35 When Output Coil ON for Reverse Running

(2) Modification of Notch Output

In Pattern B, same set values or free set-value sizes are possible as well as those in pattern A. When positionings at forward and reverse runnings are required, the pattern B is effective.

Example ; 4-notch setting

- $\overline{\text{NOTCH 0}}$ (N0) = High speed
- $\overline{\text{NOTCH 1}}$ (N1) = Middle speed
- $\overline{\text{NOTCH 2}}$ (N2) = Low speed
- $\overline{\text{NOTCH 3}}$ (N3) = Crawling speed
- $\overline{\text{NOTCH 4}}$ (N4) = Stop signal

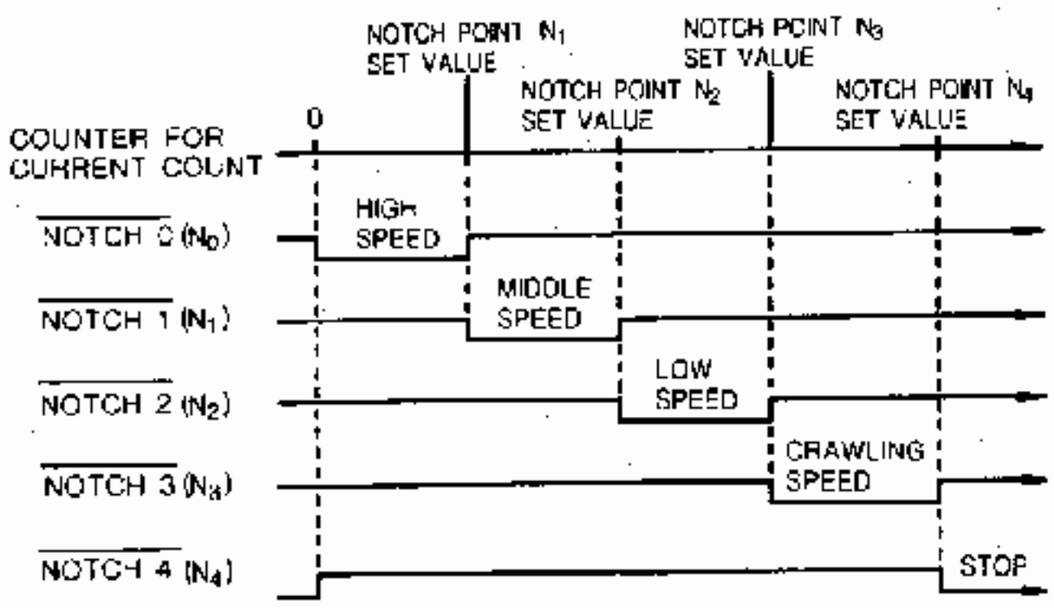


Fig. 3.36 Positioning at Forward Running: Output Coil ON

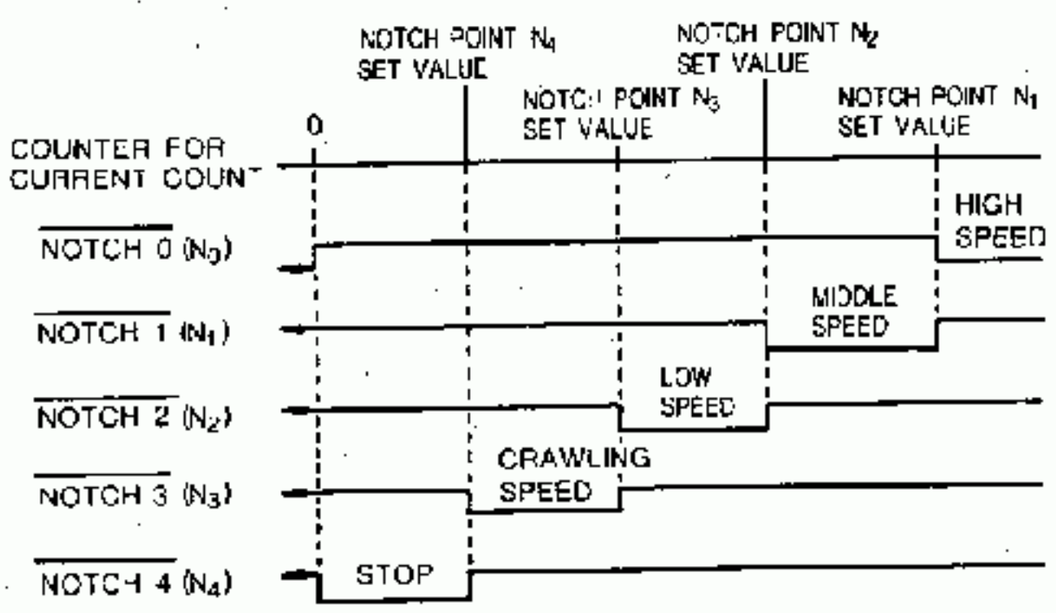


Fig. 3.37 Positioning at Reverse Running: Output Coil ON

NOTE

1. Notch output when not in use should be set to 0. In this case, the notch output results in no operation.
2. No notch output is ON until presetting notch point is done after turning power on or resetting a module.
3. In pattern B, when output coil for forward running is ON, $\overline{\text{NOTCH 0}}$ (N0) is always output while current value of the counter ranges from 0 to the least notch point set value. When output coil for reverse running is ON, $\overline{\text{NOTCH 0}}$ (N0) is always output while current value of the counter ranges from the maximum value of counter for current count to the largest notch point set value.
4. If both output coils for forward and reverse runnings are turned on, simultaneously, the coil for forward running is priority. When ENABLE output coil is ON, with both output coils for forward and reverse runnings turned off, the coil for forward running is priority. However, external $\overline{\text{forward}}$ and $\overline{\text{reverse}}$ running signals are not turned on. This concept is the same as that of hysteresis.

(3) Hysteresis Width

When the setting switch S2 is used to set the hysteresis width, a hysteresis width is given to the notch output switching process. In pattern B, when either output coil for forward or reverse running is ON, activation of hysteresis is changed.

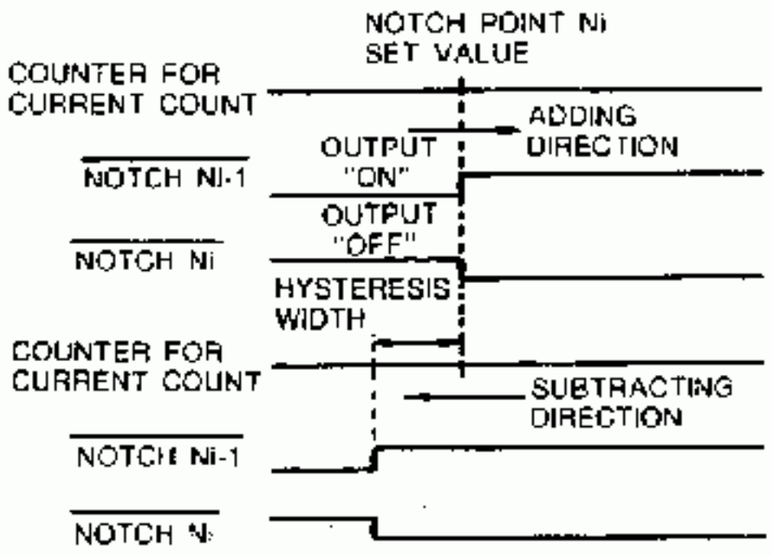
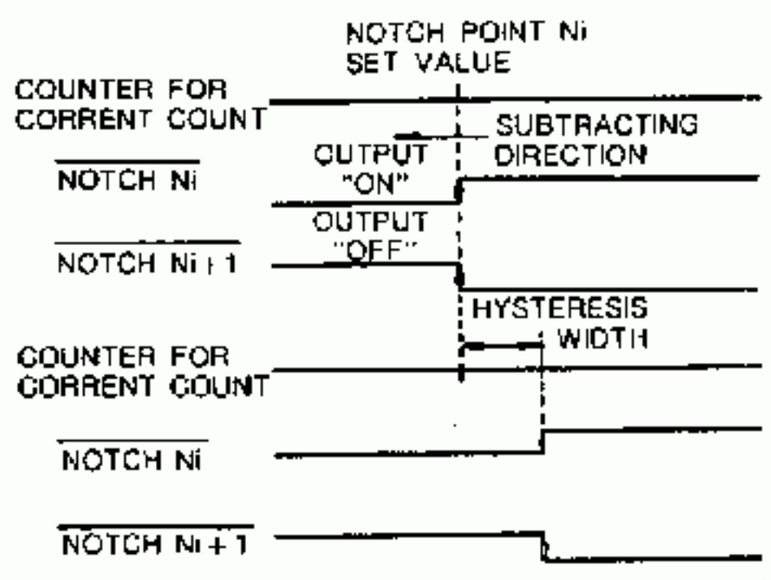


Fig. 3.38 When Output Coil ON for Forward Running

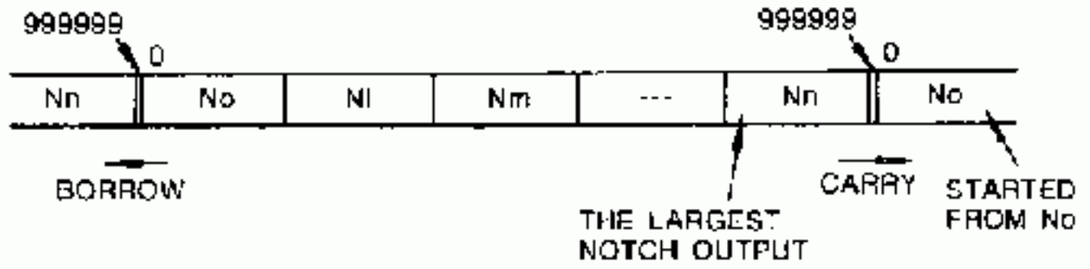


Note:
1. The hysteresis width is effective commonly to all the notch output switchings.
2. When 0 pulse is set for the hysteresis width, the width becomes zero.

Fig. 3.39 When Output Coil ON for Reverse Running

(4) Notch Output near Carry or Borrow

The notch output near CARRY and BORROW becomes endless.



Note: Hysteresis is ineffective to the notch output switching near CARRY and BORROW, even if the hysteresis width is set.

Fig. 3.40 Notch Output near Carry and Borrow

3.13 SELF DIAGNOSIS

3.13.1 Diagnostic Contents

(1) Power up diagnosis

- ROM total check
- RAM check

(2) Always

- ROM total check
- WDT check
- Bus interface time out error
- Setting format error

3. 13. 2 Procedure under Malfunctions

Table 3.17 gives procedures required under malfunction.

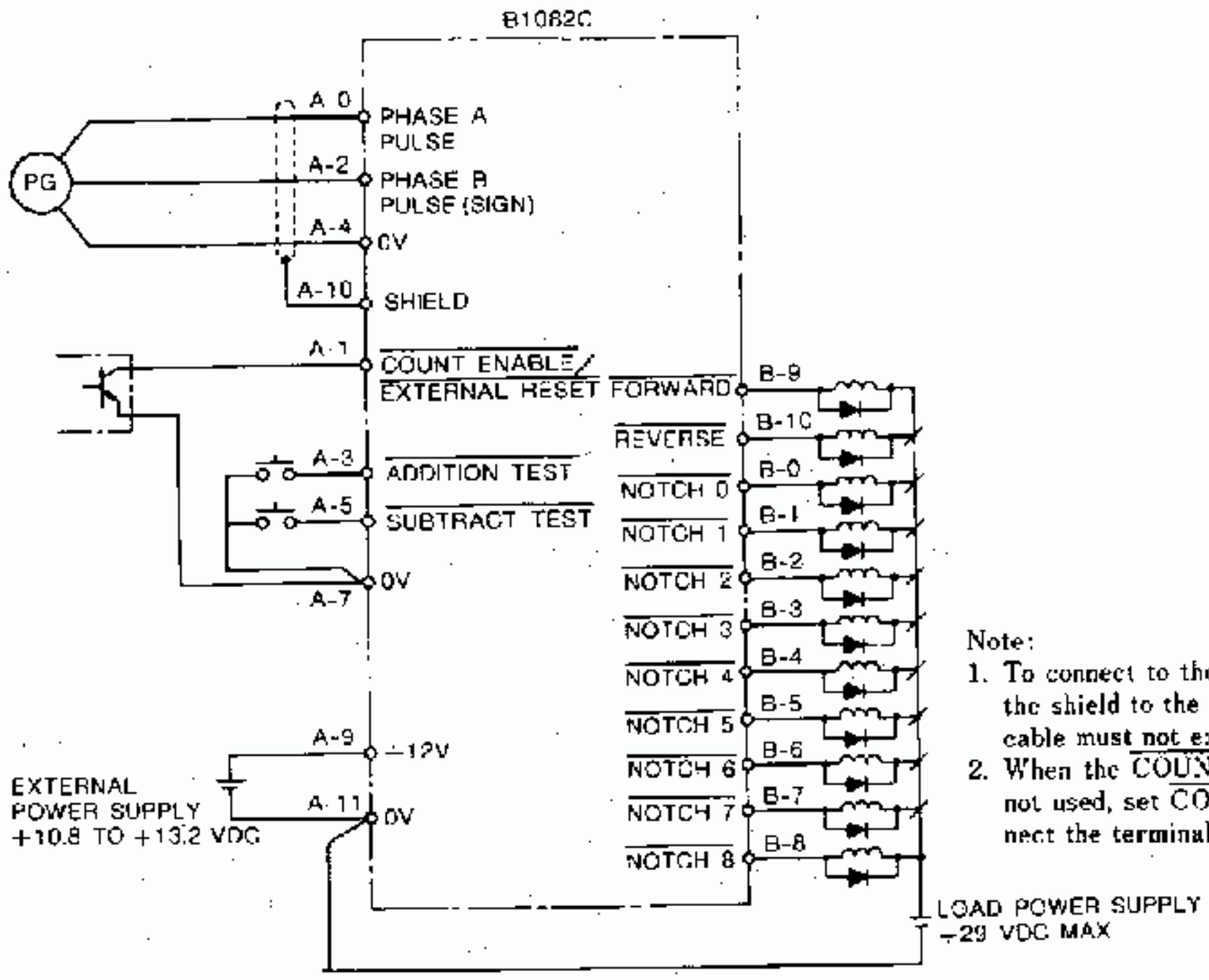
Table 3.17 Procedure under Malfunctions

Error Types	Hardware Error	Bus Interface Time out Error	Setting Format Error
Error Contents	•Those detected by self-diagnosis: [ROM total check / RAM check / WDT check] •Program running away through hardware error.	•Mainframe failure •Mainframe stopped by programming panel (PP).	•Preset reference is shorter than specified No. of scans.
ACTIVE Lamp	OFF	OFF	ON
External Output	All OFF	All OFF*	Previous output is held.
READY	OFF	ON (but no access to mainframe)	ON
ERROR	OFF	OFF (but no access to mainframe)	ON
Bus Interface	No module state as viewed from mainframe.	Disconnected	Normal
Corrective Action	When detected by self diagnosis: •Initial start by module reset. If hardware error occurs again, replace module. •For program running away, turn on and off power for initial start. If error again, replace module.	When mainframe fails, turn on and off power for initial start. When stopped by PP, start mainframe to restore	To reset ERROR, module must be reset. After resetting module, preset correctly.

*When the mainframe is stopped by PP, all the external outputs are turned off, but the counting continues. Therefore, when the mainframe is started, the current value counter's content may have changed, causing wrong notch output to be output.

Note: When the CPU is memory-cleared state, READY input relay may be OFF, but this is not error.

3. 14 EXTERNAL CONNECTION



Note:
1. To connect to the PG, be sure to use shielded cable, and connect the shield to the SHIELD terminal. As a rule, the length of PG cable must not exceed 30 meters for 40 kpps.
2. When the COUNT ENABLE/EXTERNAL RESET terminal is not used, set COUNT ENABLE by the setting switch, then connect the terminal to 0 V.

Fig. 3. 41 External Connection Diagram

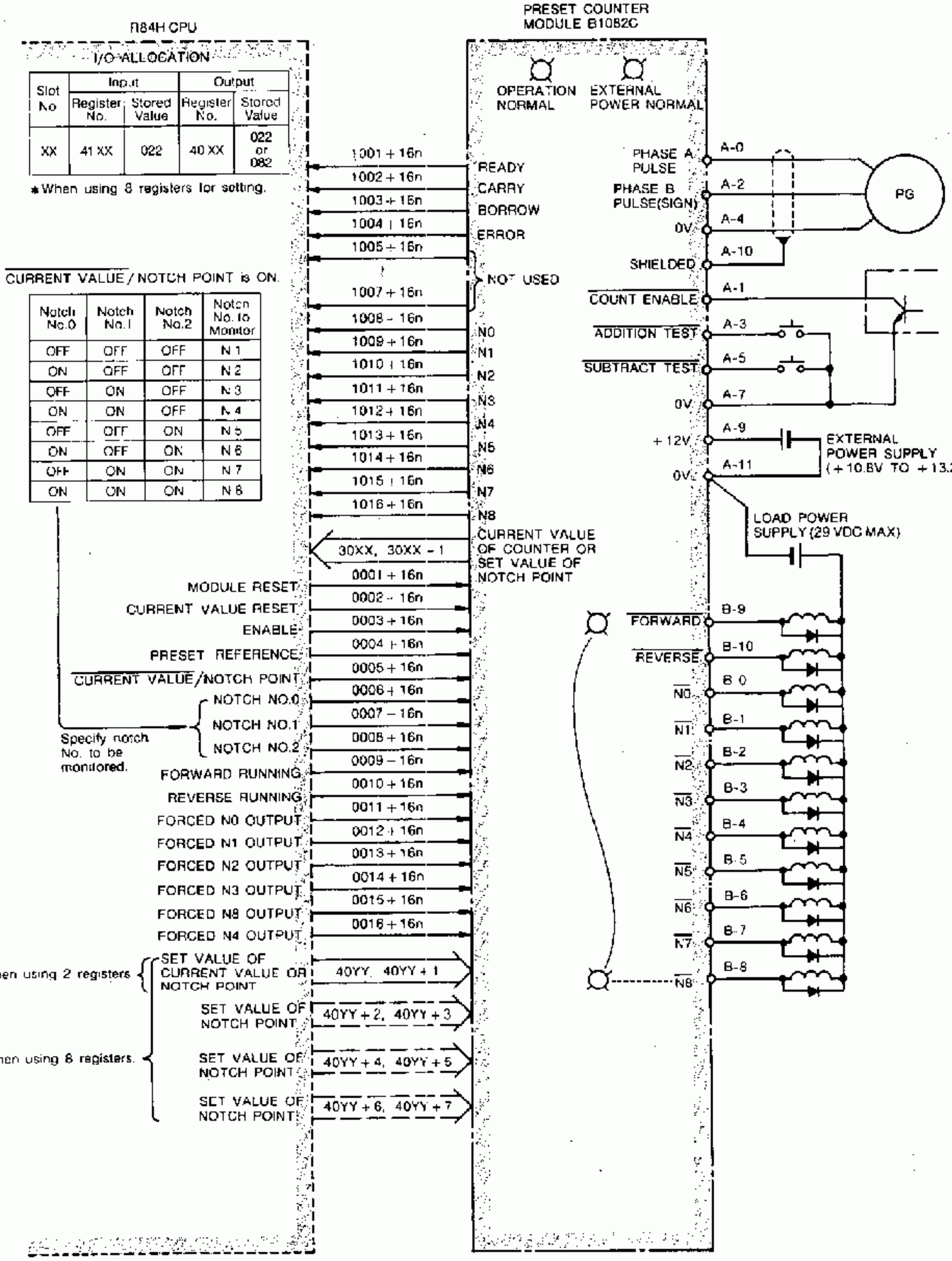
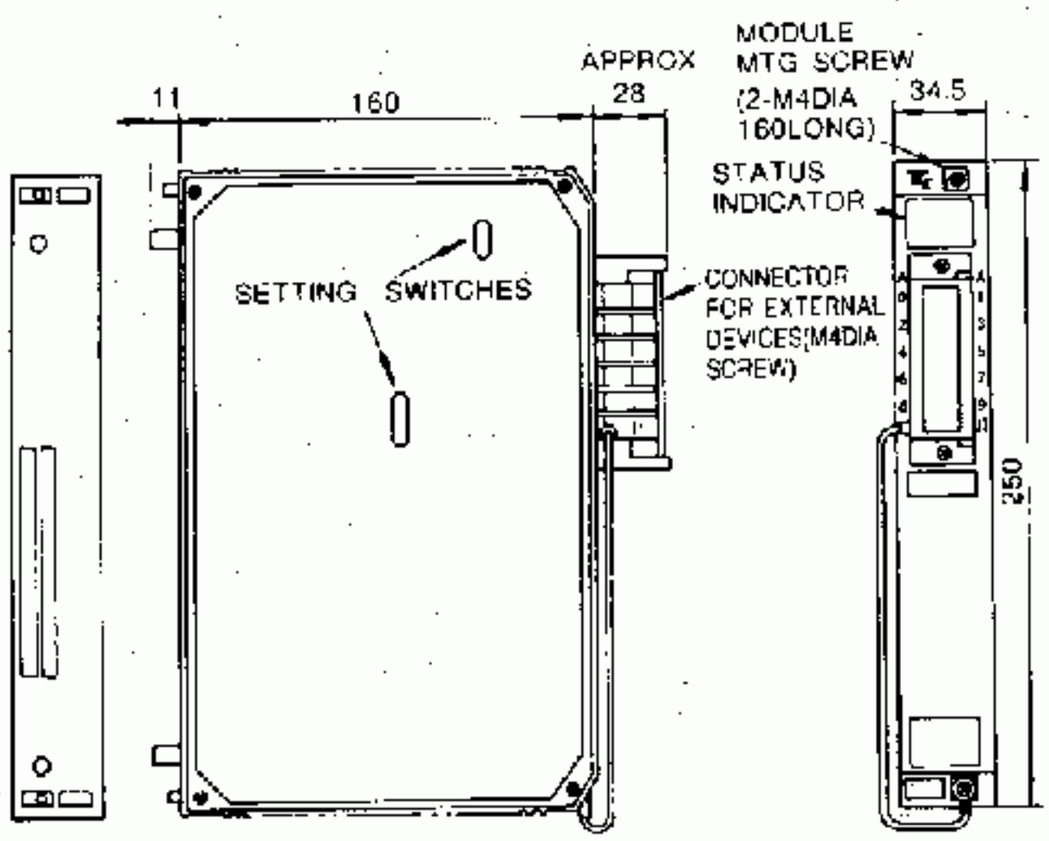


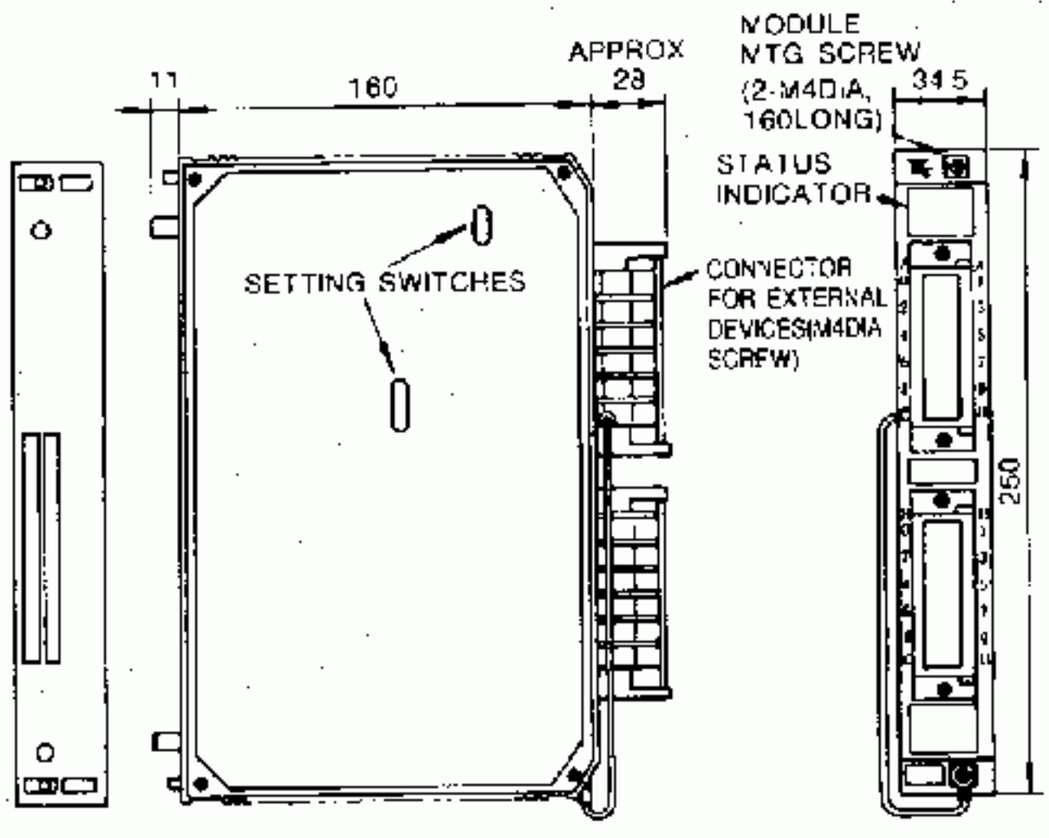
Fig. 3.42 Connection of Preset Counter Module (B1082C) and R84H

4. DIMENSIONS in mm

4.1 TYPE JAMSC-B1081C



4.2 TYPE JAMSC-B1082C



APPENDIX INPUT/OUTPUT ALLOCATION LIST (R84H)

Reversible Counter Module (B1081C)

Input / Output Allocation of *Memocon-SC* R84H	Input (41××)	Output (40××)
	021	021

Preset Counter Module (B1082C)

Input/Output Allocation of *Memocon-SC* R84H / Decimal 6 Digits	Input (41××)	Output (40××)
1-notch, 2-register×1-scan	022	022
4-notch, 2-register×4-scan	022	022
4-notch, 8-register×1-scan	022	082
8-notch, 2-register×8-scan	022	022
8-notch, 8-register×2-scan	022	082

1000 Series Counter Modules

FOR Memocon-SC R84H, U84, U84J, 584

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